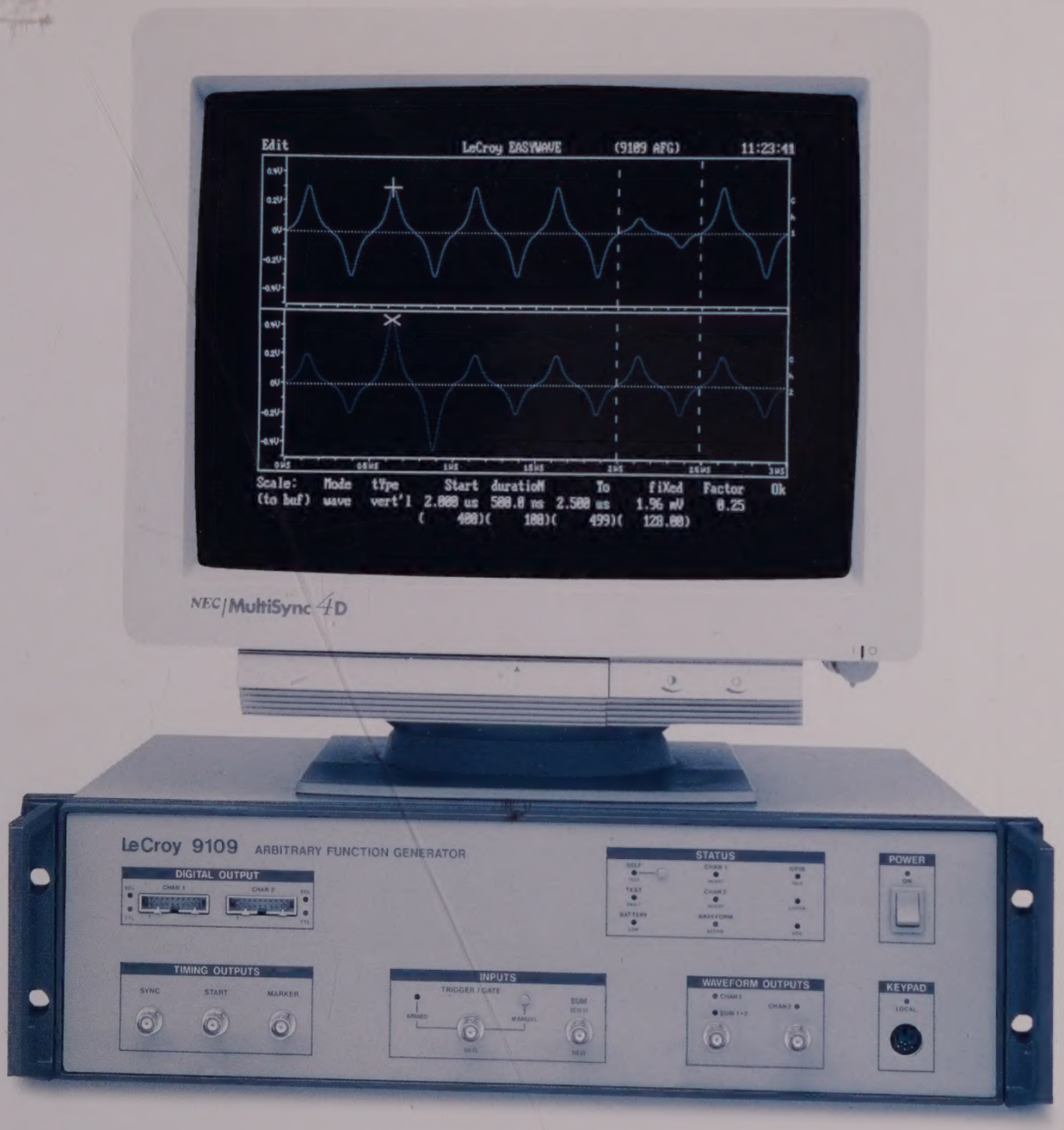
LeCroy 9100 Series Arbitrary Function Generator

Service Manual



LeCroy

Innovators in Instrumentation

9100 SERIES
ARBITRARY FUNCTION GENERATOR
SERVICE MANUAL

This manual covers the following LeCroy Arbitrary Function Generators:

9100 Dual Channel Arbitrary Function Generator
9101 Single Channel Arbitrary Function Generator
9109 Dual Channel Arbitrary Function Generator with Digital Outputs

NOVEMBER, 1988

LeCroy Corporation
700 Chestnut Ridge Road
Chestnut Ridge, NY 10977

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CHAPTER 1

GENERAL INFORMATION

1.0 Introduction

Purpose

This manual provides replaceable subassembly service information for the Model 9100 Arbitrary Function Generator.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number. Schematics are provided in Appendix C.

Unpacking and Inspection

LeCroy recommends that the shipment be thoroughly inspected immediately upon delivery. All material in the container(s) should be checked against the enclosed Packing List and shortages reported to the carrier promptly. If the shipment is damaged in any way, please notify the local LeCroy field service office. If the damage is due to mishandling during shipment, you must file a damage claim with the carrier. LeCroy 100% tests products prior to shipping. LeCroy ships all products in shipment packages designed to protect against reasonable shock and vibration.

Warranty

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations. The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

Product Assistance

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Factory headquarters, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499. Call (914) 578-6020 and ask for SSD Customer Service or call your local field service office. Additionally, SSD Customer Service has a direct phone line, (914) 578-6094.

Maintenance Agreements

LeCroy offers a selection of customer support services. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

Documentation Discrepancies

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

Software Licensing Agreement

Software products are licensed for a single machine. Under this license you may:

Copy the software for backup or modification purposes in support of your use of the software on a single machine.

Modify the software and/or merge it into another program for your use on a single machine.

Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

Service Procedure

Products requiring maintenance should be returned to an authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility.

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping.

All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department in your area.

New York Corporate Headquarters	(914) 425-6020 or
East Coast Regional Service	(914) 578-6094
New Hampshire	(603) 627-6303
Virginia	(703) 751-4148
New Mexico	(505) 293-8100
California	(415) 463-2600

Applicable Documents

LeCroy Model 9100 Operator's Manual

LeCroy Model 9100 EASYWAVE Operator's Manual

1.1 Physical Specifications

Shipping Weight: Mainframe + Manuals + Packaging: Approximately 38 lbs/17.3 kgs

Size at Furthest Points:
W 19.22 in./483 mm
D 17.22 in./437.5 mm
H 5.50 in./135.7 mm

For more dimensions, see Fig. 1-1, page 1-6.

1.2 Equipment Recommended for Service for Model 9100

The following list of equipment and accessories are needed to provide the technician access to the 9100 subassemblies during repair and calibration.

Equipment

1. 9100/CP (Control Panel)

2. 9100/SW (EASYWAVE Software)

3. IBM compatible computer; minimum 640 KB memory; with National Instruments GPIB-PC2 or equivalent GPIB interface board.

4. Frequency Counter: Phillips PM 6672/441 or equivalent counter with 35 ppm accuracy and 0.05 ppm stability

5. Oscilloscope with 0 MHz bandwidth to measure risetime

6. Digital Scope fc tes y GPIB operation with EASYWAVE software. The Le y M 9450 is recommended to fill this requirement and # abov

7. 200 MHz Pulse Generator; Tektronix FG502

8. 50 Ω ±0.1% precision feed through termination (Tektronix 011-01290-00)

9. Digital multi meter with 4 1/2 digits 0.03% accuracy, HP3468A or equivalent

Multibus Extenders are available from:

Electronic Solutions
P.O. Box 85244
San Diego, CA 92123
(619) 292-0242

Double height multibus extender 2X80EX3

SMB Barrel Connectors are available from:

Radial Connectors	Jack-to-Jack Adapter Part #R114 703

Radial Incorporated
150 Long Beach Boulevard
Stratford, CT 06497
(203) 386-1030

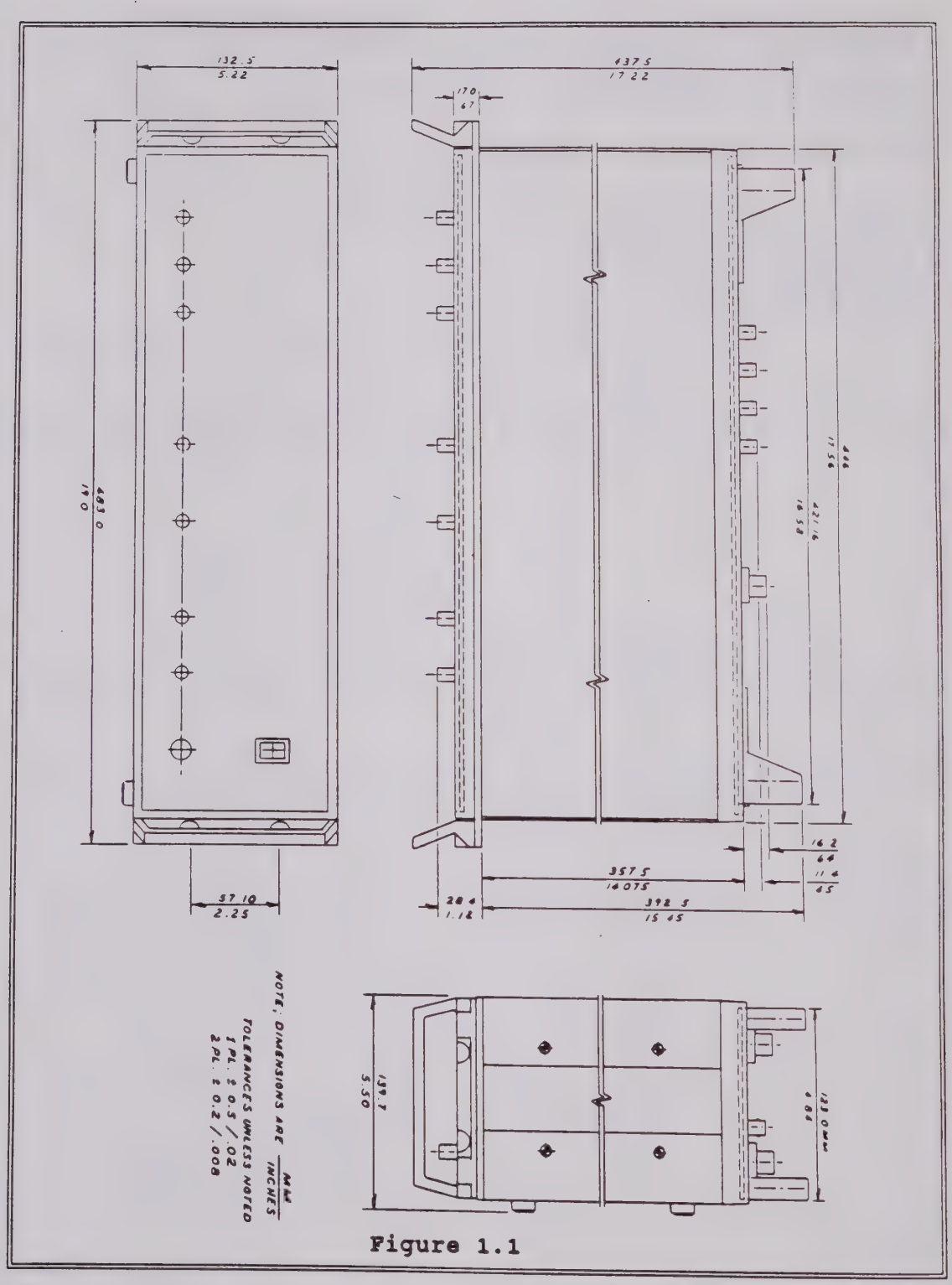

132.5
5.22
437.5
17.22
170
6.7
463.0
18.0
444
17.56
421.6
16.58
16.2
.64
11.4
.45
357.5
14.075
28.4
1.12
392.5
15.45
57.10
2.25
139.7
5.50
133.0 MM
5.24
NOTE; DIMENSIONS ARE MM / INCHES
TOLERANCES UNLESS NOTED
1 PL. ± 0.5 / .02
2 PL. ± 0.2 / .008

Figure 1.1

CHAPTER 2
INITIAL INSPECTION CRITERIA

2.0 Introduction

This chapter provides detailed procedures for use in the initial inspection of the Model 9100 using three different techniques; checking with the 9100/CP, checking with the EASYWAVE(TM) program and checking with the National Instruments IBIC program.

******** CAUTION ********

If a 9100 set for 115 V is plugged into a 220 V power source, severe damage can occur. Before powering up the unit, ensure that the correct line voltage has been set and the proper fuse is in place. The switch and fuse are located on the rear panel.

2.1 Checking Operation of the 9100/CP (Hand Held Control Panel)

EQUIPMENT REQUIRED: LeCroy 9100 AFG with 9100/CP

ACTION	RESULT
Connect the 9100/CP to the 9100 front-panel connector labeled KEYPAD, observe the Front Panel STATUS LEDs while turning the power on.	SELF TEST & WAVEFORM ACTIVE LEDs flicker. All LEDs except BATTERY LOW light briefly, but only SELF TEST remains lit. After ≈15 sec, SELF TEST turns off, the LOCAL LED above the CP connector turns on, and a blinking S appears in the lower right corner of the CP display. ≈10 sec later, the display should appear as in Figure 2-1 on the next page.

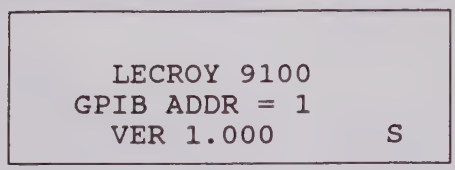


Figure 2-1
Power up display shows software version (VER) number in use and GPIB address of Model 9100 The S at the lower right blinks

Pressing [SHIFT] immediately prior to pressing a key with two functions labeled on it will initiate the upper function. Pressing [SHIFT] prior to a single function key will not initiate any command and will negate the shift instruction. To keep from storing unwanted setups in memory avoid pressing the [LEARN] key without pressing [SHIFT] first. To test the 9100/CP membrane switches listen for an audible beep with each depression. In the following list, keys marked with an asterisk (*) will initiate a display change. Ignore the messages at this time but the fact that the display changes is significant.

Press: **[F1], [F2], [F3], [F4], [FUNC]*, [CHAN1]*, [CHAN2]*,[CLOCK]*, [TRIG]*, [STATUS]*, [SHIFT], [PAGE]*, [1], [4], [7], [(-)],[LOCAL]*, [LOAD], [VIEW]*, [2], [5], [8], [0], [GO]*, [LINK], [BACK]*, [3],[6], [9], [7], [ENTER], [SHIFT], [SETUP (LEARN)].**

If an audible beep occurred after each key was depressed and the display changed when indicated then the 9100/CP is considered good.

End of 9100/CP Test.

2.2 Testing the Model 9100 with the 9100/CP

EQUIPMENT REQUIRED:

200 MHz Frequency Counter

Dual channel 100 MHz storage oscilloscope with 50 Ω input impedance or equipped with 50 Ω terminators on the inputs.

A 500 kHz 1 V p-p sinewave source with 50 Ω output.

4 equal length 50 Ω BNC coaxial cables.

Clock Outputs & Timing Outputs

ACTION	RESULT
Connect the 9100/CP to the 9100 front-panel connector labeled KEYPAD, observe the Front Panel STATUS LEDs while turning the power on.	SELF TEST & WAVEFORM ACTIVE LEDs flicker. All LEDs except BATTERY LOW light briefly, but only SELF TEST remains lit. After ≈15 sec, SELF TEST turns off, the LOCAL LED above the CP connector turns on, and a blinking S appears in the lower right corner of the CP display. ≈10 sec later, the display should appear as in Figure 2-1.
Press: **[FUNC], [F2], [F1], [GO]**	Loads & runs a single channel sinewave at default settings.
CONNECT: Rear panel CLOCK OUT 1 to frequency counter.	Frequency counter reads 200 MHz ± 400 Hz.
DISCONNECT: CLOCK OUT 1.	
CONNECT: Rear panel CLOCK OUT 2 to frequency counter.	Frequency counter reads 200 MHz ± 400 Hz.
DISCONNECT: CLOCK OUT 2.	

SET OSCILLOSCOPE TO: .5 µS/div
Channel 1: 1 V/div 50 Ω DC coupled
Channel 2: N/A
Trig: AC coupled
Source: Channel 1
Slope: Positive
Sweep Mode: Normal

ACTION	RESULT
CONNECT: LeCroy 9100 START output to oscilloscope channel 1.	
Adjust oscilloscope trigger level.	A series of 1.5 V pulses, ≈25 nS wide and 1 μS apart will appear on scope (See Figure 2-2).

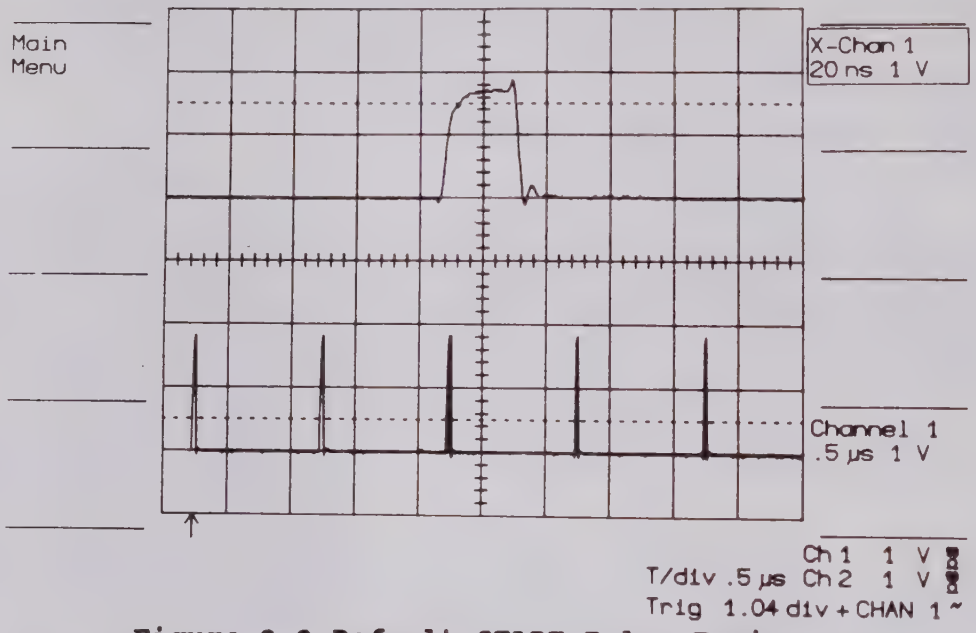


Figure 2-2 Default START Pulse Train

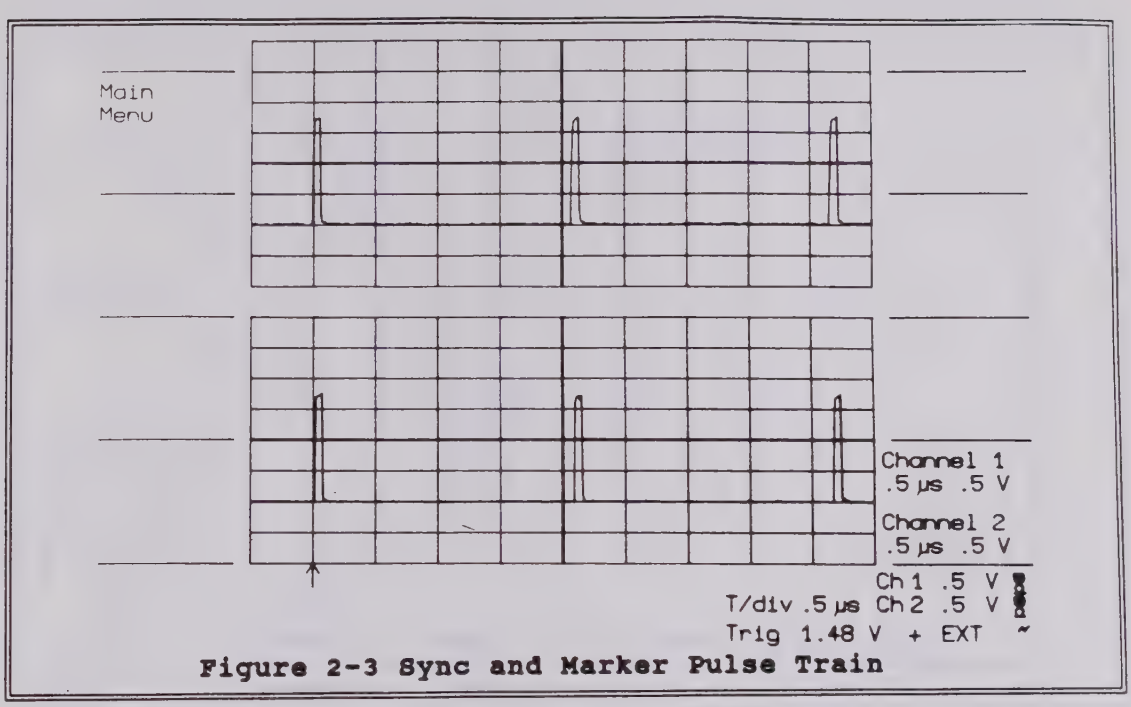


Figure 2-3 Sync and Marker Pulse Train

ACTION	RESULT
SET OSCILLOSCOPE TO: Channel 1: .5 V .5 µS 50 Ω dc Channel 2: .5 V .5 µS 50 Ω dc Trig: AC coupled Source: External Slope: Positive	
CONNECT: LeCroy 9100 START output to scope external trigger in; SYNC output to scope Channel 1; MARKER output to Channel 2.	
Press: **[TRIG], [F1], [F2], [2], [ENTER]** Adjust scope trigger level.	Trigger mode changes to recurrent, with 2 repetitions. Each channel displays a series of 1.5 V pulses, ≈100 nS wide, and 2.1 µS apart (see Fig. 2-3).

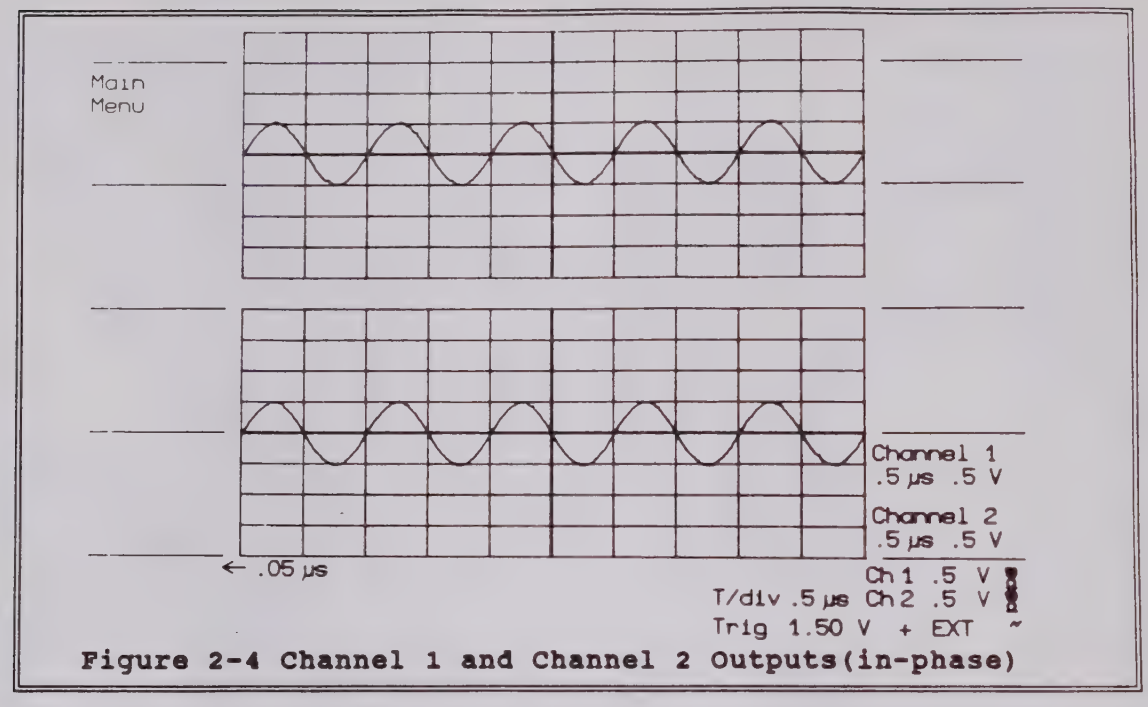


Figure 2-4 Channel 1 and Channel 2 Outputs(in-phase)

Waveform Outputs

ACTION	RESULT
Press: **[TRIG], [F1], [F1], [FUNC], [F2], [F1], [F1]**	Loads & runs a dual channel sinewave in continuous mode.
CONNECT: LeCroy 9100 CHAN 1 output to scope Channel 1; CHAN 2 output to scope Channel 2	Scope displays a pair of in phase sinewaves, 1 V p-p, with a 1 µS period (see Figure 2-4).

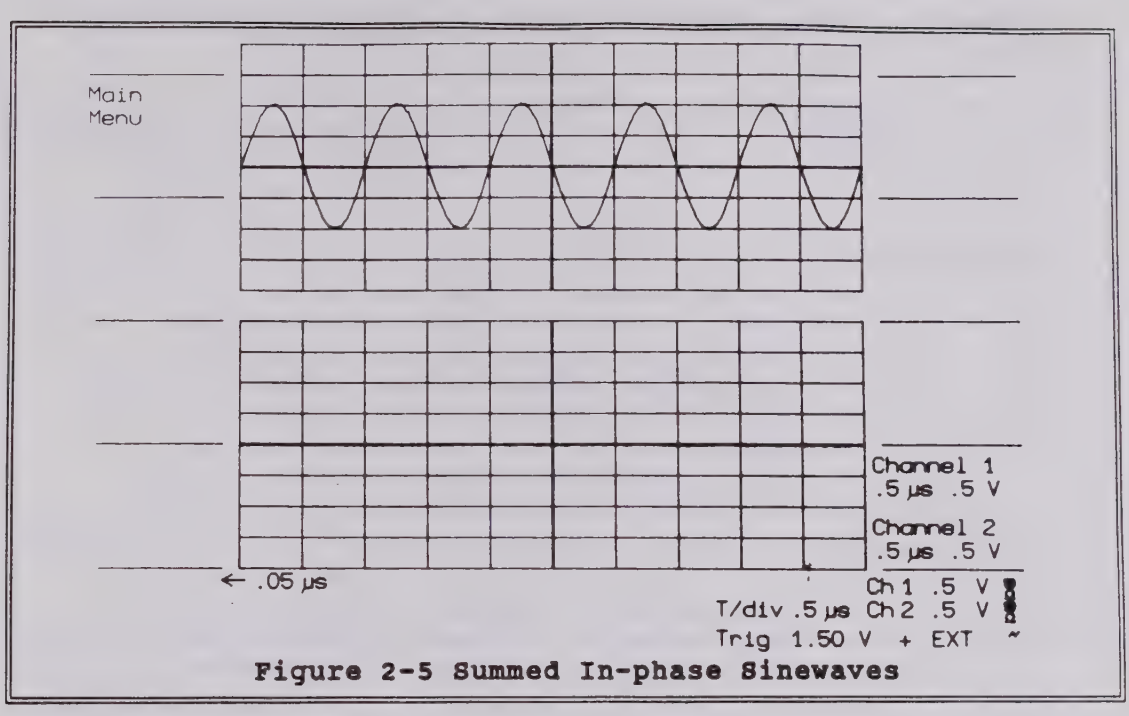


Figure 2-5 Summed In-phase Sinewaves

ACTION	RESULT
Press: **[CHAN 1], [PAGE], [F3]**	WAVEFORM OUTPUTS sections CHAN 2 LED goes out and SUM 1+2 comes on. 9100 internally sums channels 1 and 2 to create a 2 V p-p sinewave (see Figure 2-5).
Press: **[F3]**	CHAN 2 LED comes on. SUM 1+2 LED goes off. Waveform appears as in Figure 2-4.
DISCONNECT: CHAN 2 output from oscilloscope.	
CONNECT: CHAN 2 output to the INPUTS section SUM BNC.	
Press: **[F4]**	Waveform appears as in Figure 2-5.
DISCONNECT: CHAN 2 output from the SUM input.	

ACTION	RESULT
CONNECT: CHAN 2 output to scope Chan 2 Input.	Waveform appears as in Figure 2-4.
Press: **[F4] [CHAN 1], [PAGE], [F2]**	STATUS section CHAN 1 INVERT LED comes on, channel 1's output is 180° out of phase as in Figure 2-6.

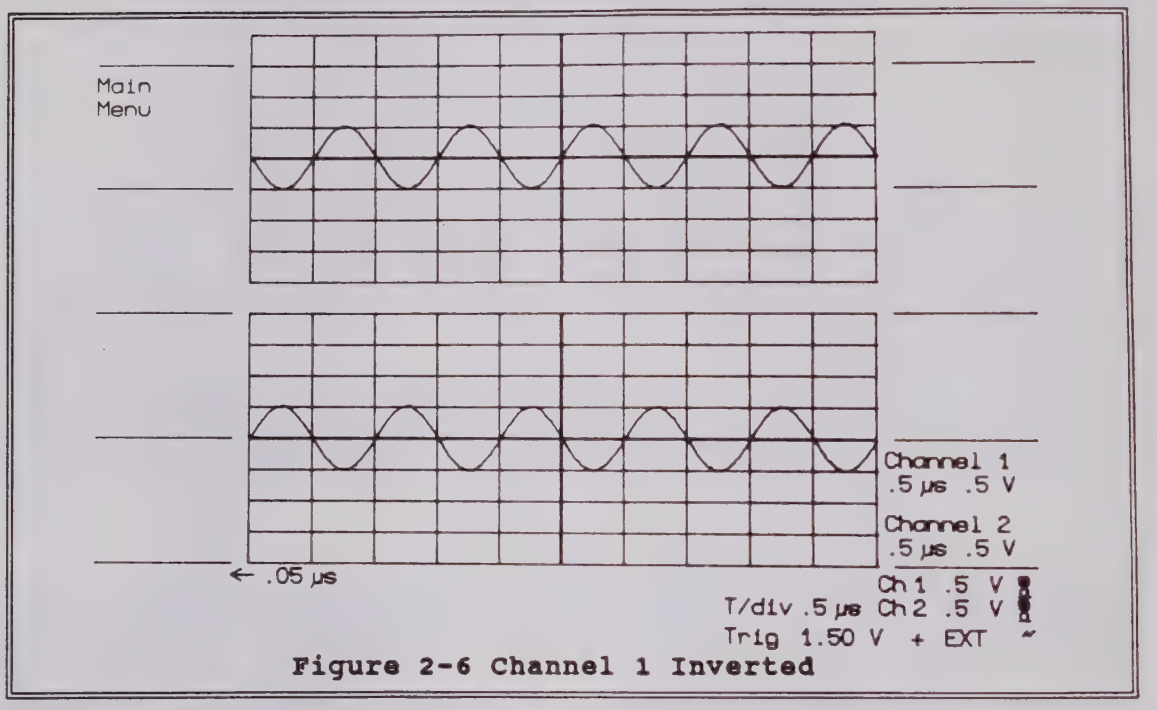


Figure 2-6 Channel 1 Inverted

Press: **[F2]**	CHAN 1 INVERT LED goes out. Sinewaves are in phase as in Figure 2-4.

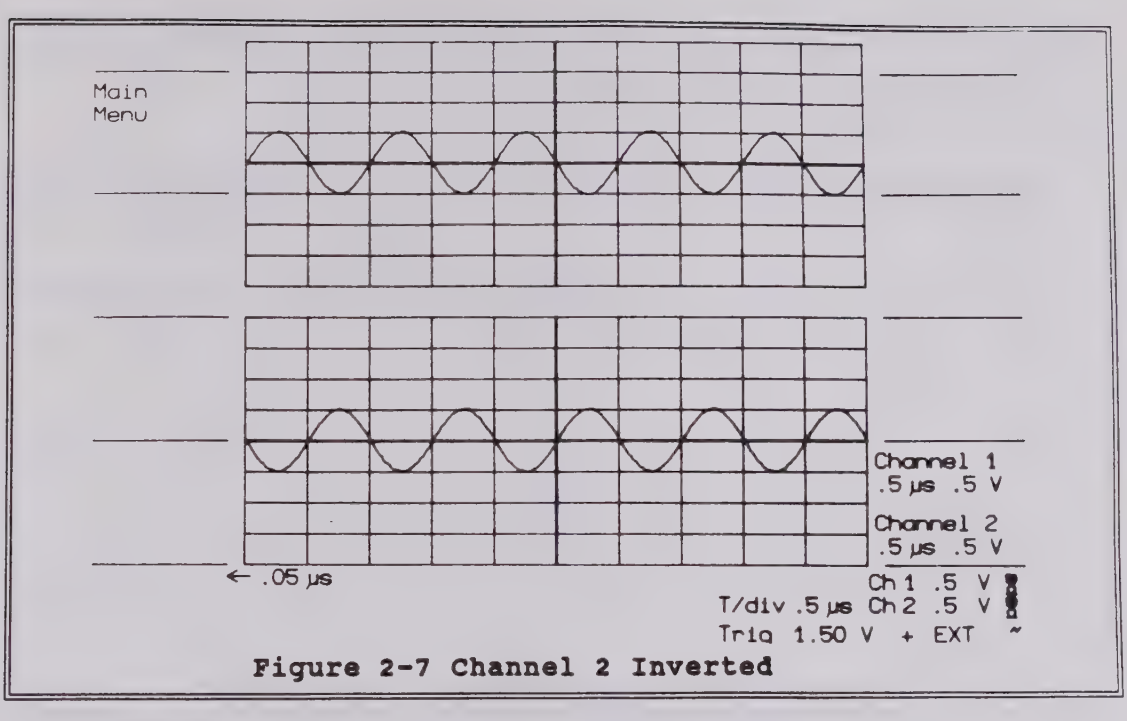


Figure 2-7 Channel 2 Inverted

ACTION	RESULT
Press: **[Chan 2], [PAGE], [F2]**	CHAN 2 INVERT LED comes on, channel 2's output is 180° out of phase as in Figure 2-7.
Press: **[F2]**	CHAN 2 INVERT LED goes out, sinewaves are in phase as in Figure 2-4.
Press: **[TRIG], [F1], [PAGE], [F1], [TRIG], [PAGE], [F3], [.], [2], [SHIFT], [V]**	Changes trigger mode to gated, with a 200 mV threshhold level.

SET OSCILLOSCOPE TO: 1 µsec/div

SET AN EXTERNAL SIGNAL SOURCE FOR:
500 kHz 1 V p-p sinewave.

CONNECT: 9100 SYNC output to scope external trigger input.

CONNECT: TRIGGER/GATE input to SIGNAL SOURCE output	STATUS section ARMED LED flashes on and off.

ACTION	RESULT
CONNECT: 9100 CHAN 1 output to scope channel 1	
CONNECT: 9100 CHAN 2 output to scope channel 2	Scope displays a series of 1 μS/cycle sinewaves, separated in time by 1 μS as in Figure 2-8.

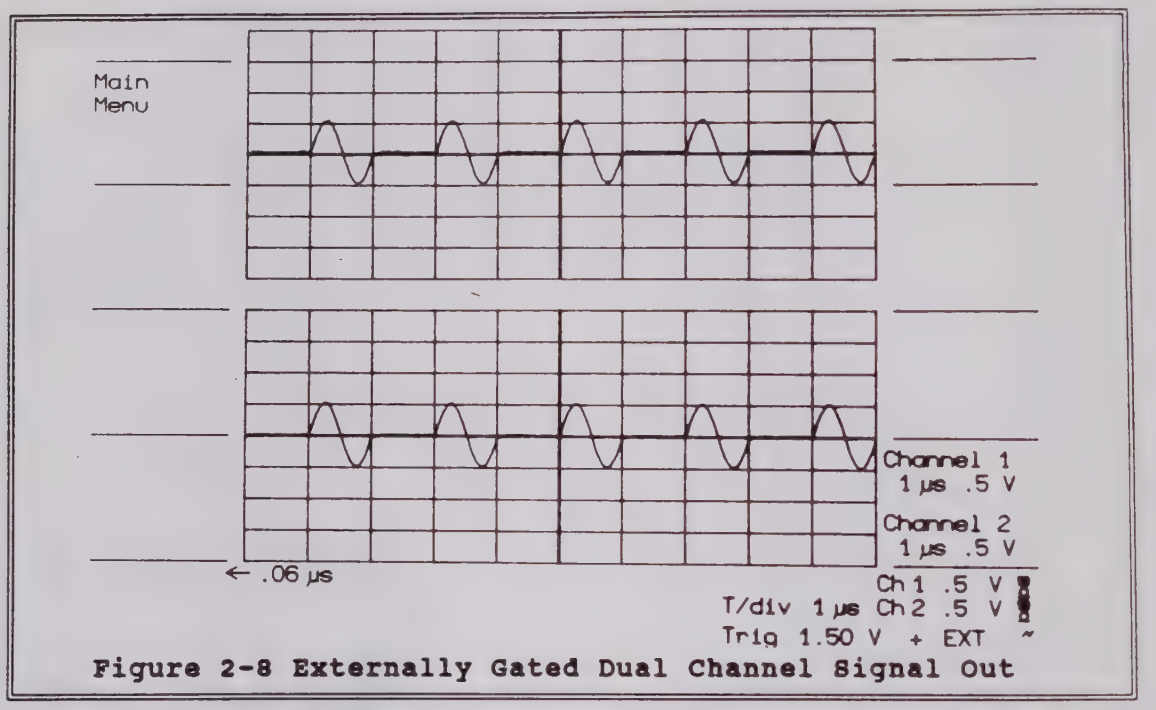


Figure 2-8 Externally Gated Dual Channel Signal Out

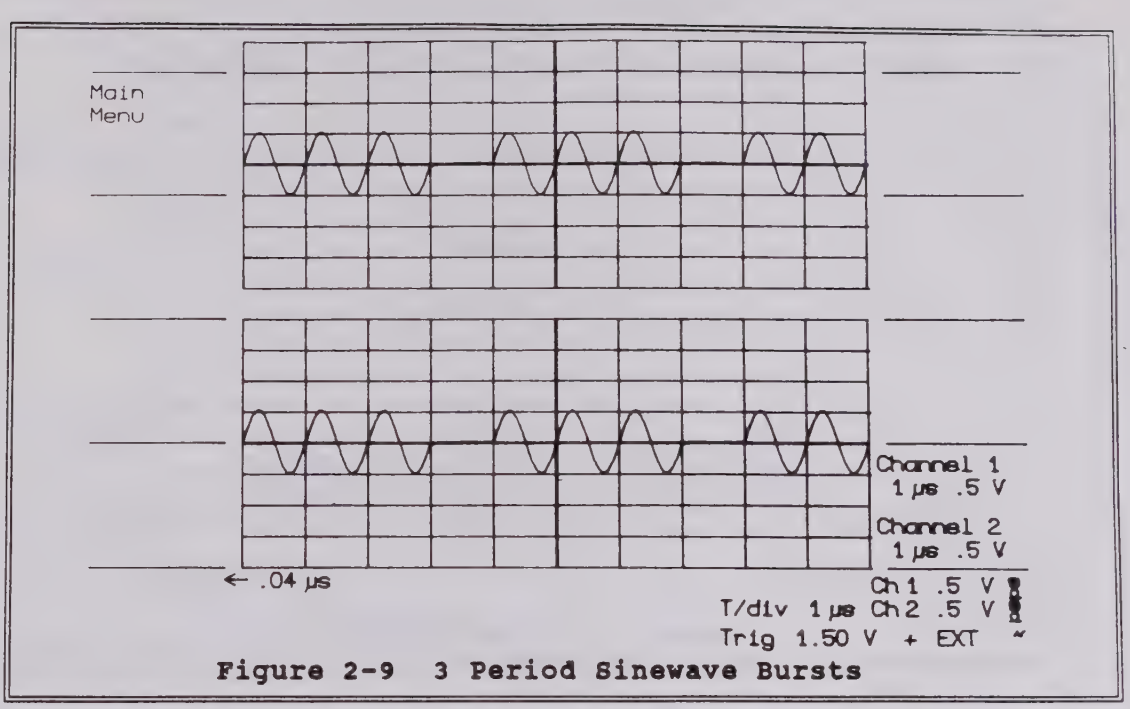


Figure 2-9 3 Period Sinewave Bursts

ACTION	RESULT
Press: **[TRIG],[F1],[F4],[3], [ENTER], [TRIG], [PAGE], [F1], [F2]**	Bursts of 3 sinewaves appear, each burst separated in time from the previous by 1 µS, as in Figure 2-9, ARMED LED continues to flash.
Press: **[TRIG],[F1],[F3]**	Changes trigger mode to single. Waveform appears as in Figure 2-8. ARMED LED continues to flash.
DISCONNECT: The external signal from the TRIGGER/GATE BNC.	ARMED LED stays on. Channel 1 output ceases.
SET OSCILLOSCOPE TO: Single-shot Storage mode	
Press: INPUTS section MANUAL button.	A single cycle of a sinewave 1 µS long occurs for each push of the MANUAL button. See Figure 2-10.

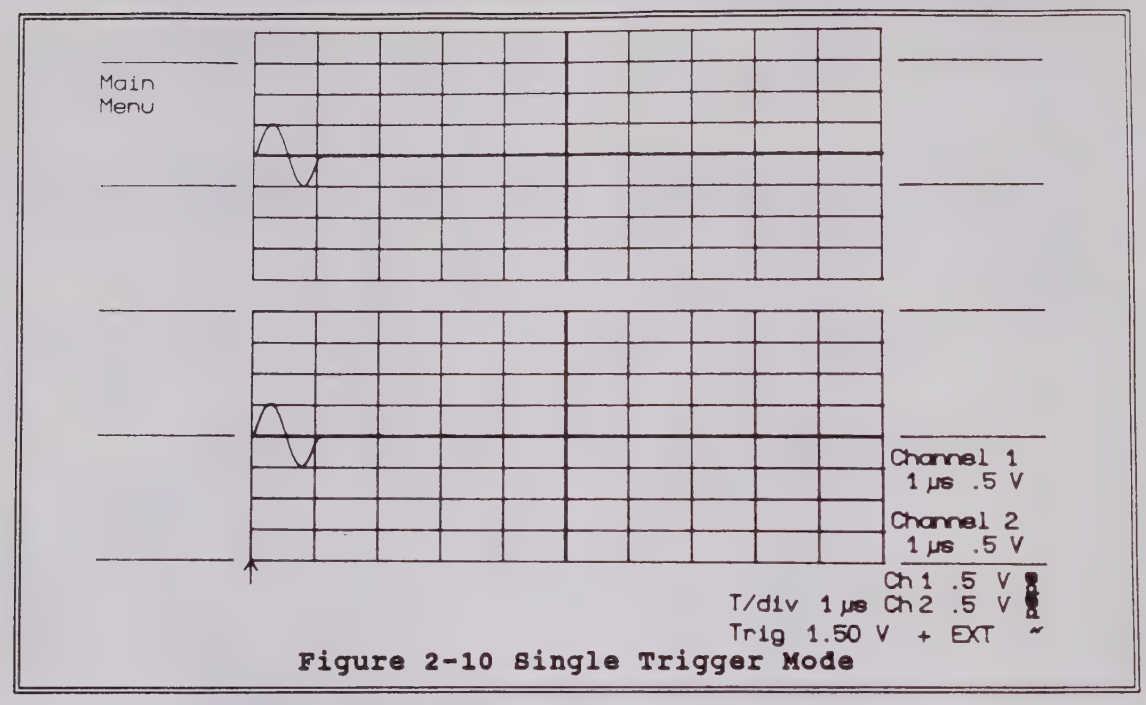


Figure 2-10 Single Trigger Mode

RAM Storage Battery Test

NOTE: Although the battery backed up storage should last for greater than two months, this test will fail if the battery has not been fully charged or the 9100 has not been used for an extended amount of time. In such cases it may be necessary to let the battery charge for approximately three hours before performing this test.

ACTION	RESULT
Press: **[SHIFT], [RESET], [F3]**	9100 resets to power-up state. Control Panel display looks like Figure 2-1.
SET OSCILLOSCOPE TO: Non-Storage Mode.	
Press: **[FUNC], [F2], [F1], [F2], [5], [0], [0], [SHIFT], [KHz], [GO]**	A 500 kHz, 1 V p-p sinewave appears on Channel 1.
Press: **[LEARN]**	The 9100/CP display appears as in Figure 2-11 with "XXX" being any number from 1-999 depending on how many setup files are stored. The R in the lower right hand corner

of the display should be blinking.

WRITE DOWN THE SET NUMBER FOR FUTURE REFERENCE!

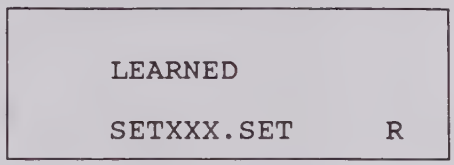


Figure 2-11 Learned Setup Display
The R at the lower right blinks

ACTION	RESULT
Turn the 9100 power off for approximately two minutes.	
Turn Power ON, wait for the power-up display (Figure 2-1) to appear.	9100 powers up in default state.
Press: **[FUNC], [F3]**	
If the SETUP number recorded is not displayed, press **[PAGE]** until it is.	
Press: the Function Key **[F1], [F2], [F3], or [F4]** that corresponds to the line of the display the recorded SETUP number is on, then **[SHIFT], [SETUP]**.	9100/CP display appears as in Figure 2-12a (next page), with XXX being the SETUP number.

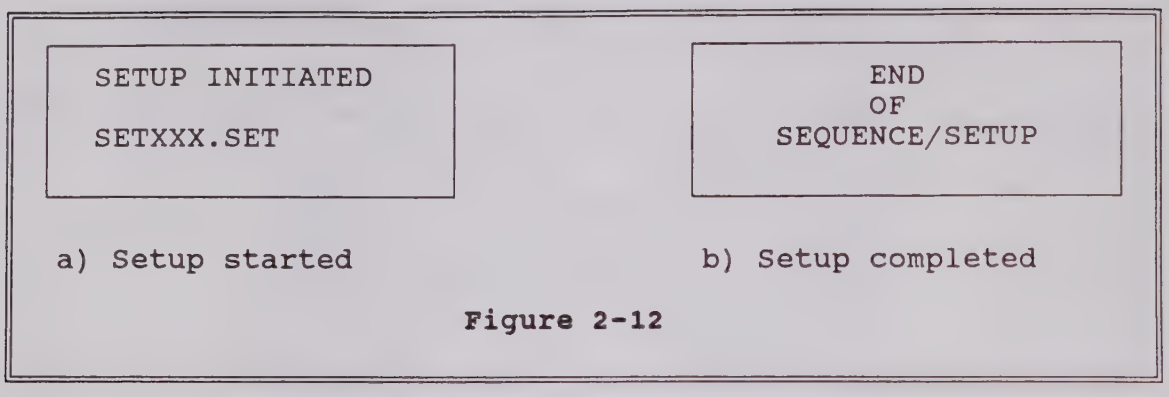


Figure 2-12

ACTION	RESULT
Press: **[FUNC], [F2], [F1], [GO]**	500 KHz 1 V p-p sinewave appears on Channel 1

2.3 Testing the Model 9100 with EASYWAVE Software

EQUIPMENT REQUIRED:

IBM PC with National Instruments GPIB Interface Adaptor Model PC2 or PC2A.

Dual channel 100 MHz storage oscilloscope with 50 Ω input impedance or equipped with 50 Ω terminators on the inputs.

A 500 kHz 1 V p-p sinewave source with 50 Ω output.

4 equal length 50 Ω BNC coaxial cables.

Load the EASYWAVE program into the computer according to the EASYWAVE Operator's Manual. Once you are in the program follow the directions below for setting up the LeCroy 9100. Note that the carriage return (peformed using the "ENTER" key on most IBM PC compatible computers) will not always be used except while in an editing menu. The command will be executed immediately upon pressing the desired command key. In the case where multiple commands are given it is not always necessary to wait for the next EASYWAVE menu screen to come up.

Clock Outputs & Timing Outputs

ACTION	RESULT
Observe the front-panel Status LEDs while turning the power on	SELF TEST & WAVEFORM ACTIVE LEDs flicker. All LEDs except BATTERY LOW light briefly, but only SELF TEST remains lit. After ≈15 sec, SELF TEST turns off, and about 10 sec later the LOCAL LED above the CP connector turns on.
Type: **O F S A G**	Loads & runs a single channel sinewave at default settings.
CONNECT: Rear panel CLOCK OUT 1 to frequency counter.	Frequency counter reads 200 MHz ± 400 Hz.
DISCONNECT: CLOCK OUT 1.	
CONNECT: Rear panel CLOCK OUT 2 to frequency counter.	Frequency counter reads 200 MHz ± 400 Hz.
DISCONNECT: CLOCK OUT 2.	

SET OSCILLOSCOPE TO: .5 μS/div
Channel 1: 1 V/div 50 Ω DC coupled
Channel 2: N/A
Trig: AC coupled
Source: Channel 1
Slope: Positive
Sweep Mode: Normal

CONNECT: LeCroy 9100 START output to oscilloscope channel 1.	
Adjust oscilloscope trigger level.	A series of 1.5 V pulses, ≈25 nS wide and 1 μS apart will appear on scope (See Figure 2-13).

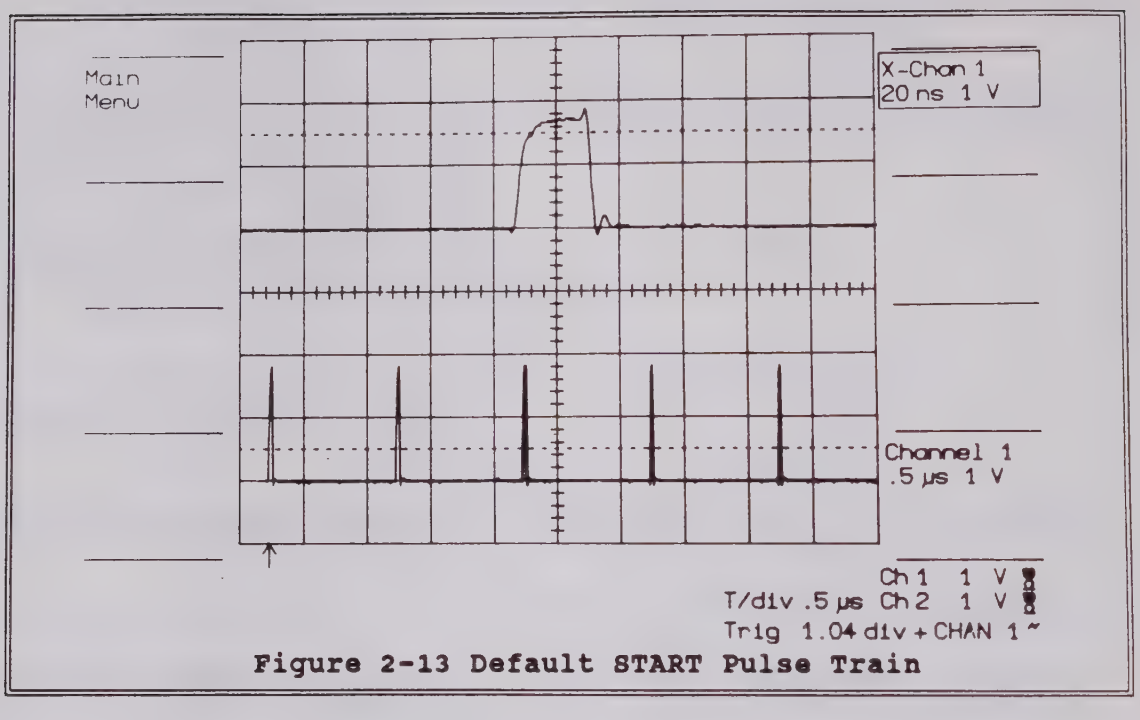


Figure 2-13 Default START Pulse Train

ACTION	RESULT
SET OSCILLOSCOPE TO: Channel 1: .5 V .5 µS 50 Ω dc Channel 2: .5 V .5 µS 50 Ω dc Trig: AC coupled Source: External Slope: Positive	
CONNECT: LeCroy 9100 START output to scope external trigger in; SYNC output to scope Channel 1; MARKER output to Channel 2.	
Type: **<Esc> S <right arrow> <down arrow> R 2 <Enter>.** Adjust scope trigger level.	Trigger mode changes to recurrent, with 2 repetitions. Each channel displays a series of 1.5 V pulses, ≈100 nS wide, and 2.1 µS apart (see Fig. 2-14, next page).

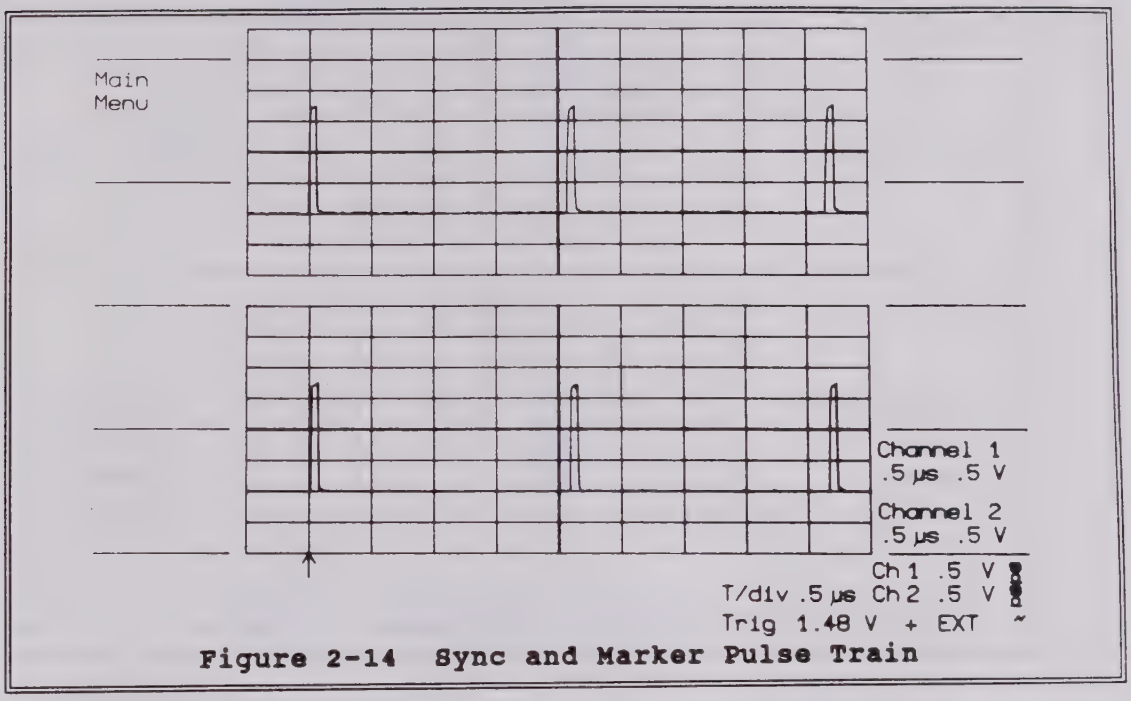


Figure 2-14 Sync and Marker Pulse Train

Waveform Outputs

ACTION	RESULT
Type: **<Esc> M S <right arrow> <down arrow> C**	Loads & runs a dual channel sinewave in continuous mode.
CONNECT: LeCroy 9100 CHAN 1 output to scope Channel 1;	Scope displays a pair of in phase sinewaves, 1 V p-p, CHAN 2 output to scope Channel 2 with a 1 µS period (see Figure 2-15).

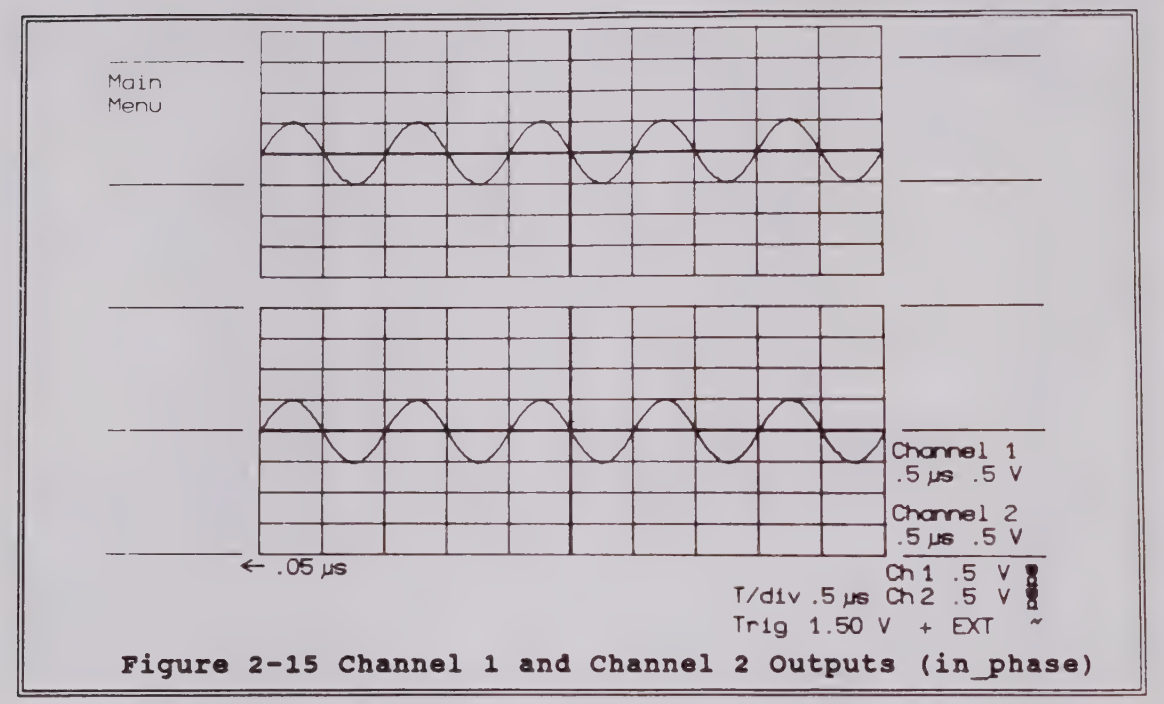


Figure 2-15 Channel 1 and Channel 2 Outputs (in_phase)

ACTION	RESULT
Type: **<left arrow> <up arrow> <spacebar>**	WAVEFORM OUTPUTS sections CHAN 2 LED goes out and SUM 1+2 comes on. 9100 internally sums channels 1 and 2 to create a 2 V p-p sinewave (see Figure 2-16, next page).

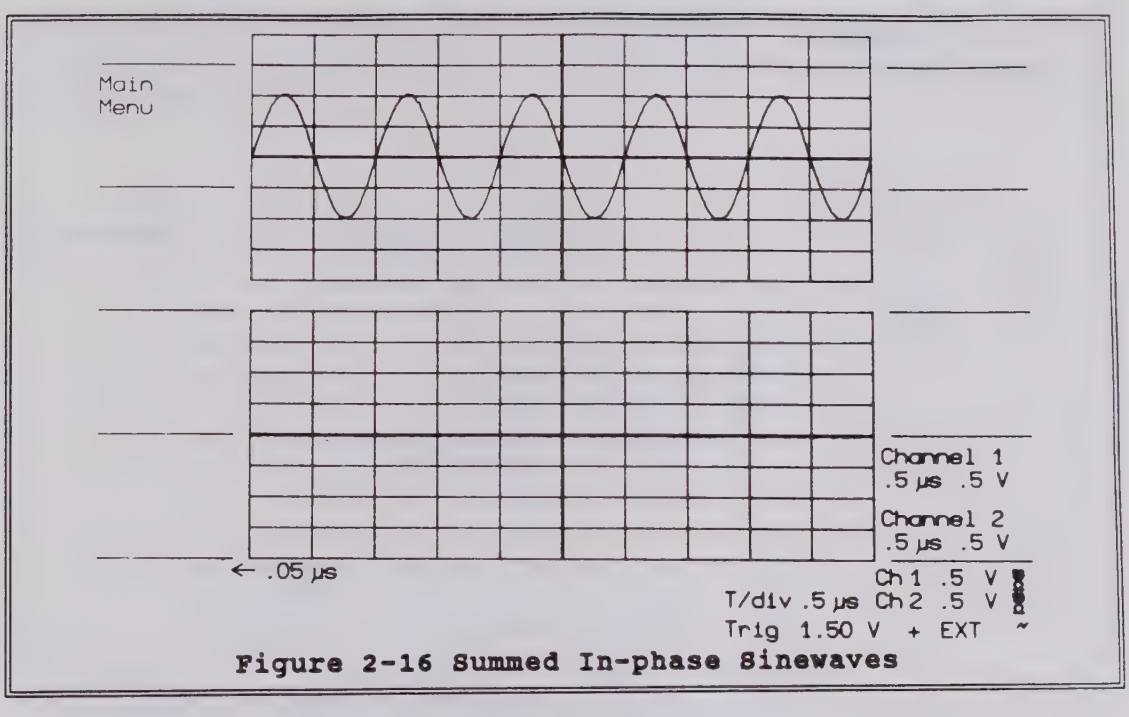


Figure 2-16 Summed In-phase Sinewaves

ACTION	RESULT
Type: **<spacebar>**	CHAN 2 LED comes on. SUM 1+2 LED goes off. Waveform appears as in Figure 2-15.
DISCONNECT: CHAN 2 output from oscilloscope.	
CONNECT: CHAN 2 output to the INPUTS section SUM BNC.	
Type: **<down arrow> <spacebar>**	Waveform appears as in Figure 2-16.
DISCONNECT: CHAN 2 output from the SUM input.	
CONNECT: CHAN 2 output to scope Chan 2 Input.	Waveform appears as in Figure 2-15.

ACTION	RESULT
Type: **<spacebar> <up arrow> <up arrow> <spacebar>**	STATUS section CHAN 1 INVERT LED comes on, channel 1's output is 180° out of phase as in Figure 2-17.

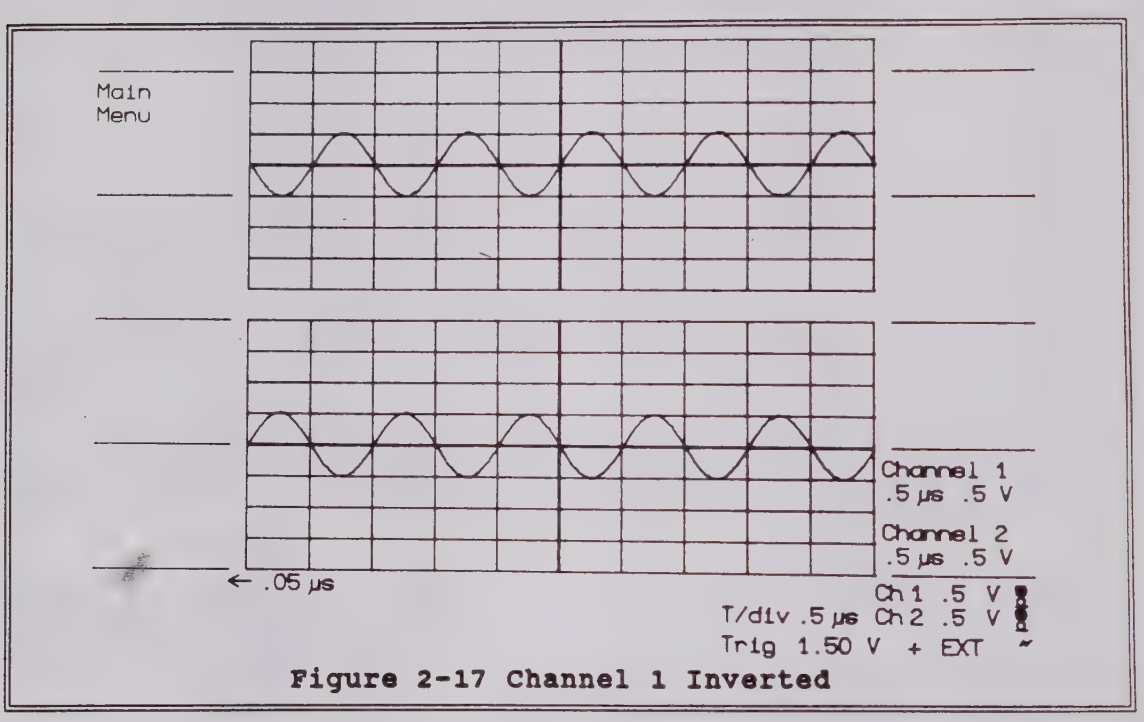


Figure 2-17 Channel 1 Inverted

Type: **<spacebar>**	CHAN 1 INVERT LED goes out. Sinewaves are in phase as in Figure 2-15.
Type: **<down arrow> <down arrow> <down arrow> <down arrow> <down arrow> <down arrow> <down arrow> <down arrow> <spacebar>**	CHAN 2 INVERT LED comes on, channel 2's output is 180° out of phase as in Figure 2-18.

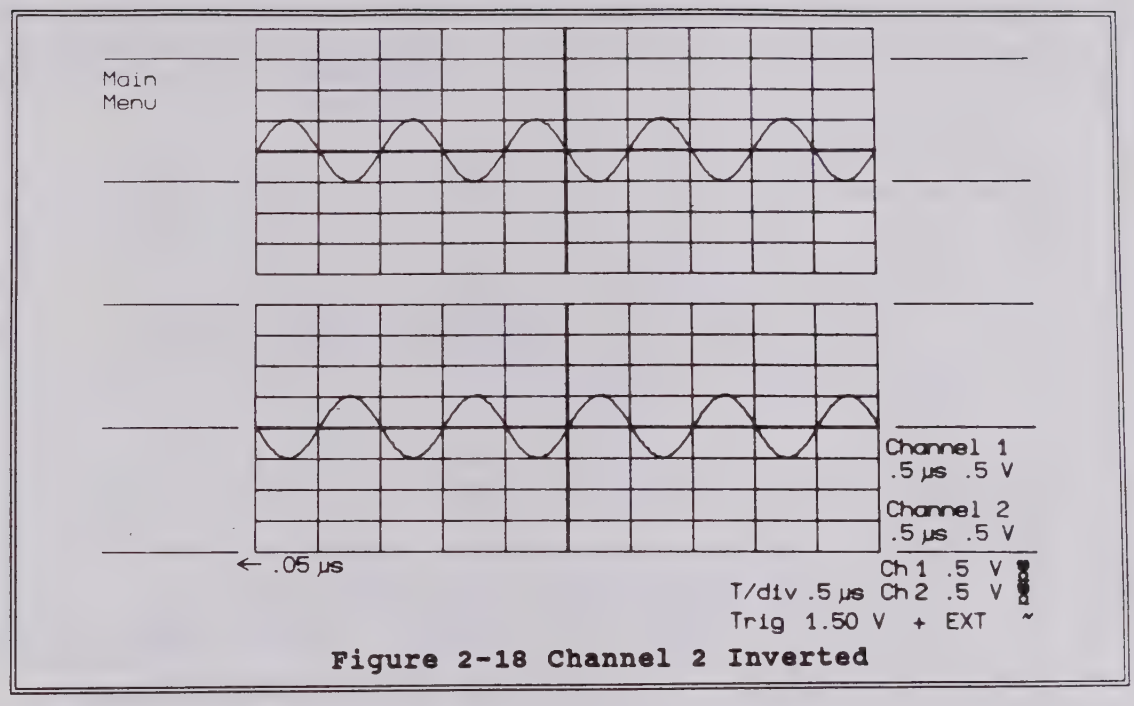


Figure 2-18 Channel 2 Inverted

ACTION	RESULT
Type: **<spacebar>**	CHAN 2 INVERT LED goes out, sinewaves are in phase as in Figure 2-15.
Type: **<right arrow> G** **<down arrow> 200 mV** **<Enter>**	Changes trigger mode to gated, with a 200 mV threshhold level.
SET OSCILLOSCOPE TO: 1 µsec/div	
SET EXTERNAL SIGNAL SOURCE FOR: 500 kHz 1 V p-p sinewave.	
CONNECT: 9100 SYNC output to scope external trigger input.	
CONNECT: TRIGGER/GATE input to SIGNAL SOURCE output	STATUS section ARMED LED flashes on and off.
CONNECT: 9100 CHAN 1 output to scope channel 1	

ACTION	RESULT
CONNECT: 9100 CHAN 2 output to scope channel 2	Scope displays a series of 1 μsec/cycle sinewaves, separated in time by 1 μsec as in Figure 2-19.

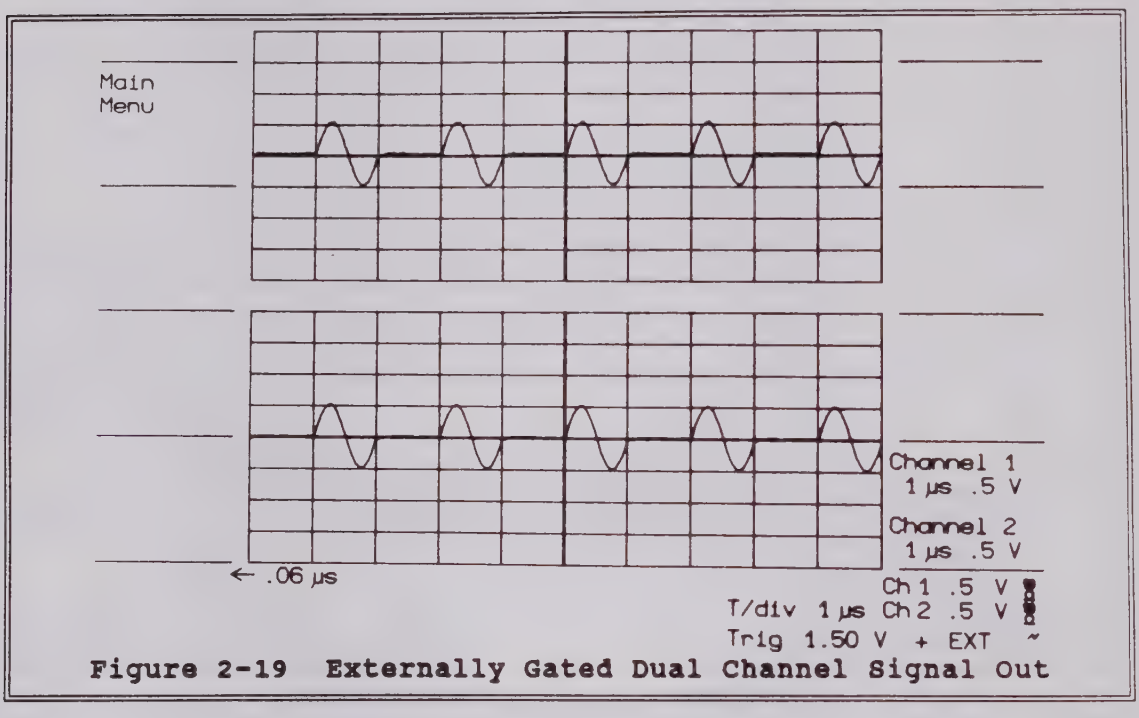


Figure 2-19 Externally Gated Dual Channel Signal Out

Type: **<up arrow> B 3 <Enter> <down arrow> <down arrow> <down arrow> <spacebar>**	Bursts of 3 sinewaves appear, each burst separated in time from the previous by 1 μS, as in Figure 2-20, next page. ARMED LED continues to flash.

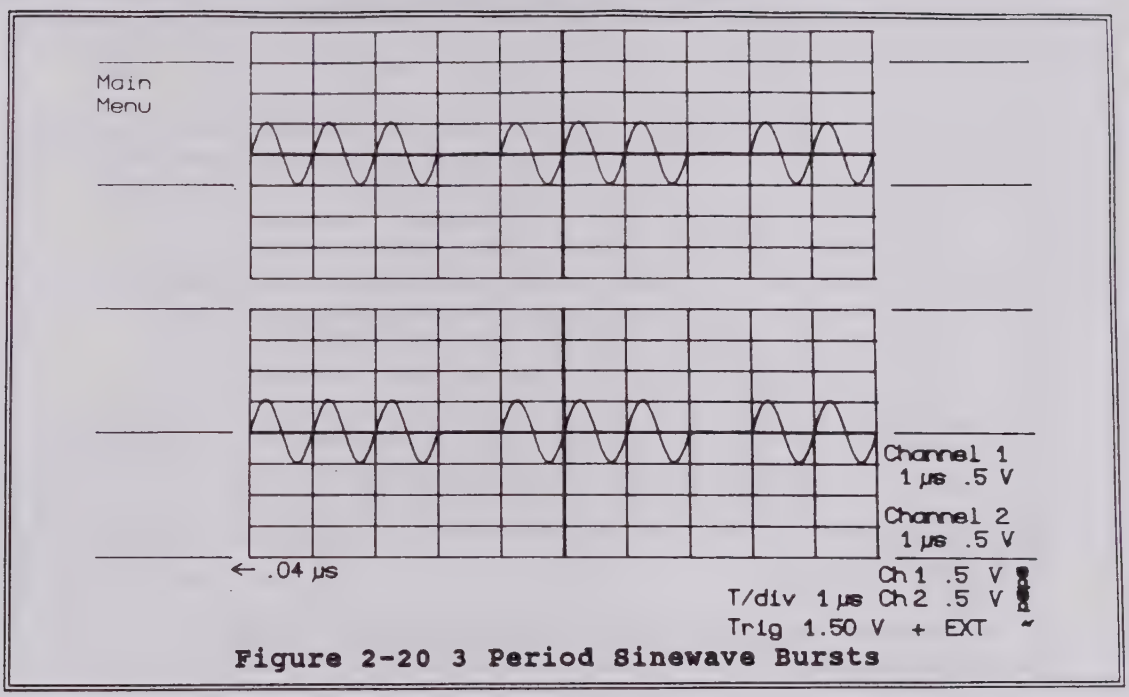


Figure 2-20 3 Period Sinewave Bursts

ACTION	RESULT
Type: **<up arrow> <up arrow> <up arrow> S**	Changes trigger mode to single. ARMED LED remains lit. Channel 1 output ceases.
DISCONNECT: The external signal from the TRIGGER/GATE BNC.	
Type: **<F4> <F2> Y**	Exit Easywave, return to local control.
SET OSCILLOSCOPE TO: Single-shot Storage mode	
Press: INPUTS section MANUAL button.	A single cycle of a sinewave 1 µS long occurs for each push of the MANUAL button. See Figure 2-21.

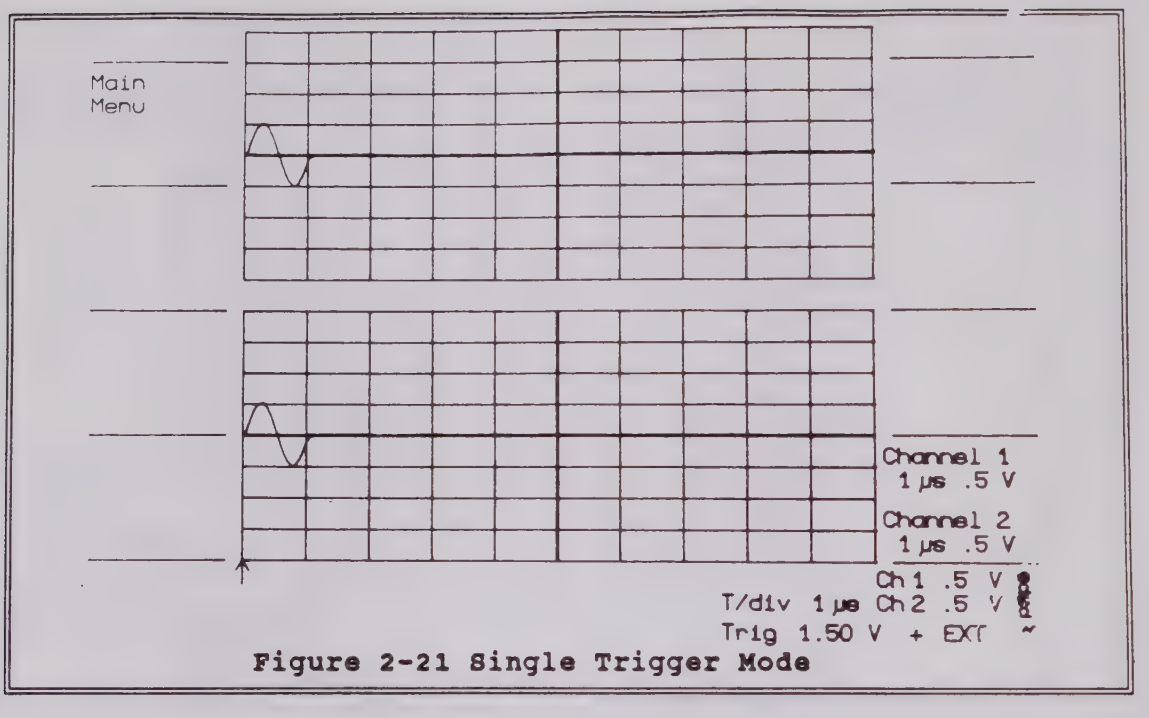


Figure 2-21 Single Trigger Mode

RAM Storage Battery Test

NOTE: Although the battery backed up storage should last for greater than two months, this test will fail if the battery has not been fully charged or the 9100 has not been used for an extended amount of time. In such cases it may be necessary to let the battery charge for approximately three hours before performing this test.

ACTION	RESULT
Type: **ew <Enter>**	Re-start Easywave program
Type: **O F S M S 2 <Enter>** **<down arrow> <down arrow>** **<down arrow> <down arrow>** **<down arrow> <down arrow>** **<down arrow> <down arrow>** **3 <Enter> <down arrow>** **<down arrow> <down arrow>** **<down arrow> <down arrow>** **<down arrow> <down arrow>** **R3 <Enter> <up arrow>** **<up arrow> <up arrow>** **50 <Enter> <Esc> A G <Esc>** **R RECUR <Enter>**	Load a standard, dual-channel sinewave, @ 1 MHz. Change Channel 1 amplitude to 2 V p-p, Channel 2 amplitude to 3 V p-p, and trigger mode to recurrent with 3 repetitions, and a 50 point trigger delay. When started (by the 'G') the output should appear as in Figure 2-22 (next page). The remaining commands store the current AFG settings in the 9100's RAM-disk under the filename Recur.set.

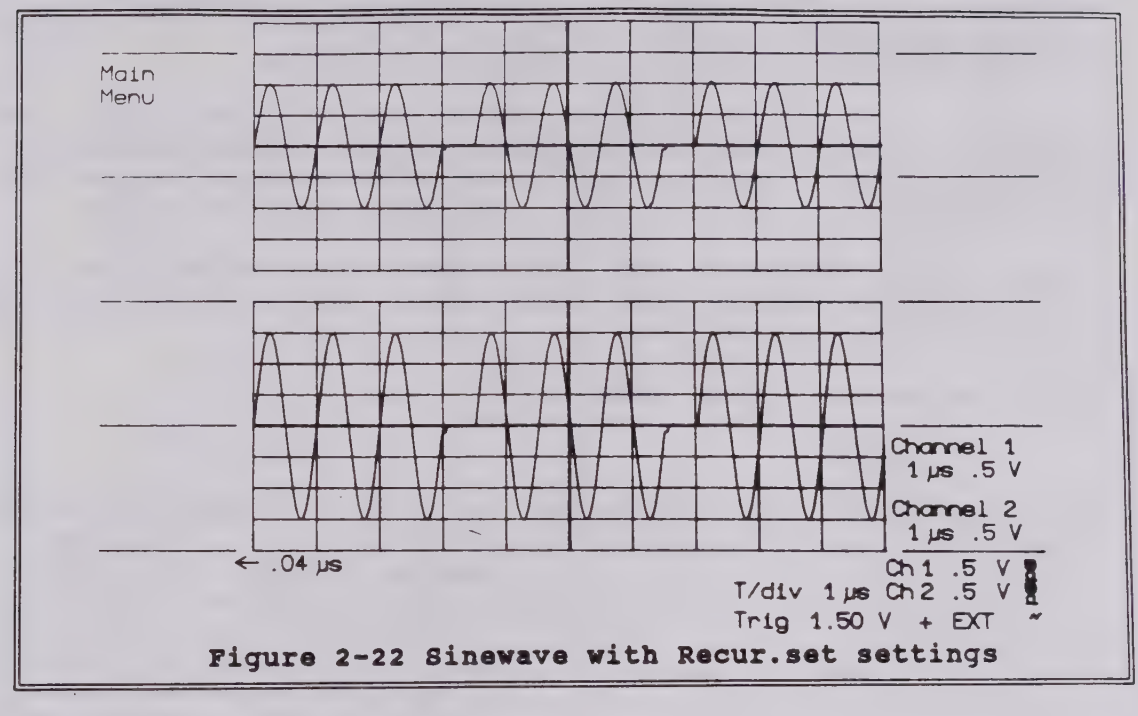


Figure 2-22 Sinewave with Recur.set settings

ACTION	RESULT
After the Settings file has been learned, turn the 9100's power off for about 2 minutes.	Easywave will report that it has lost communication with AFG & return to System Menu.
Re-apply power to 9100 & wait for LOCAL LED to light.	
Type: **O F S A S RECUR <Enter> G**	Waveform appears as in Figure 2-22.

2.4 Testing the 9100 Using National Instruments Software

EQUIPMENT REQUIRED:

IBM PC with National Instruments GPIB Interface Adaptor Model PC2 or PC2A.

Dual channel 100 MHz storage oscilloscope with 50 Ω input impedance or equipped with 50 Ω terminators on the inputs.

A 500 kHz 1 V p-p sinewave source with 50 Ω output.

4 equal length 50 Ω BNC coaxial cables.

The following test uses National Instruments hardware and software, including the IBIC program. IBIC is used because it keeps the commands simple and it is included with the purchase of the GPIB package from National Instruments.

Connect the LeCroy 9100 GPIB port to the computer. Load the IBIC program into the computer and follow the procedure outlined below. **<ENTER>** must be used to execute the commands. Use quotation marks to contain the commands to the 9100.

Type: **ibfind <Enter>.** The IBIC program will prompt you to type in the device name at this time. Enter the name you gave the board in your IBCONF file.

Clock Outputs & Timing Outputs

ACTION	RESULT
Observe the front-panel Status LEDs while turning the power on	SELF TEST & WAVEFORM ACTIVE LEDs flicker. All LEDs except BATTERY LOW light briefly, but only SELF TEST remains lit. After ≈15 sec, SELF TEST turns off, and about 10 sec later, the LOCAL LED above the CP connector turns on.
Type: **ibwrt <Enter> "sine;" <Enter> ibwrt <Enter> "go;" <Enter>**	Loads & runs a single channel sinewave at default settings.
CONNECT: Rear panel CLOCK OUT 1 to frequency counter.	Frequency counter reads 200 MHz ± 400 Hz.
DISCONNECT: CLOCK OUT 1.	
CONNECT: Rear panel CLOCK OUT 2 to frequency counter.	Frequency counter reads 200 MHz ± 400 Hz.
DISCONNECT: CLOCK OUT 2.	

SET OSCILLOSCOPE TO: .5 μS/div
Channel 1: 1 V/div 50 Ω DC coupled
Channel 2: N/A
Trig: AC coupled
Source: Channel 1
Slope: Positive
Sweep Mode: Normal

CONNECT: LeCroy 9100 START output to oscilloscope channel 1.

Adjust oscilloscope trigger level.

A series of 1.5 V pulses, ≈25 nS wide and 1 μS apart will appear on scope (See Figure 2-23).

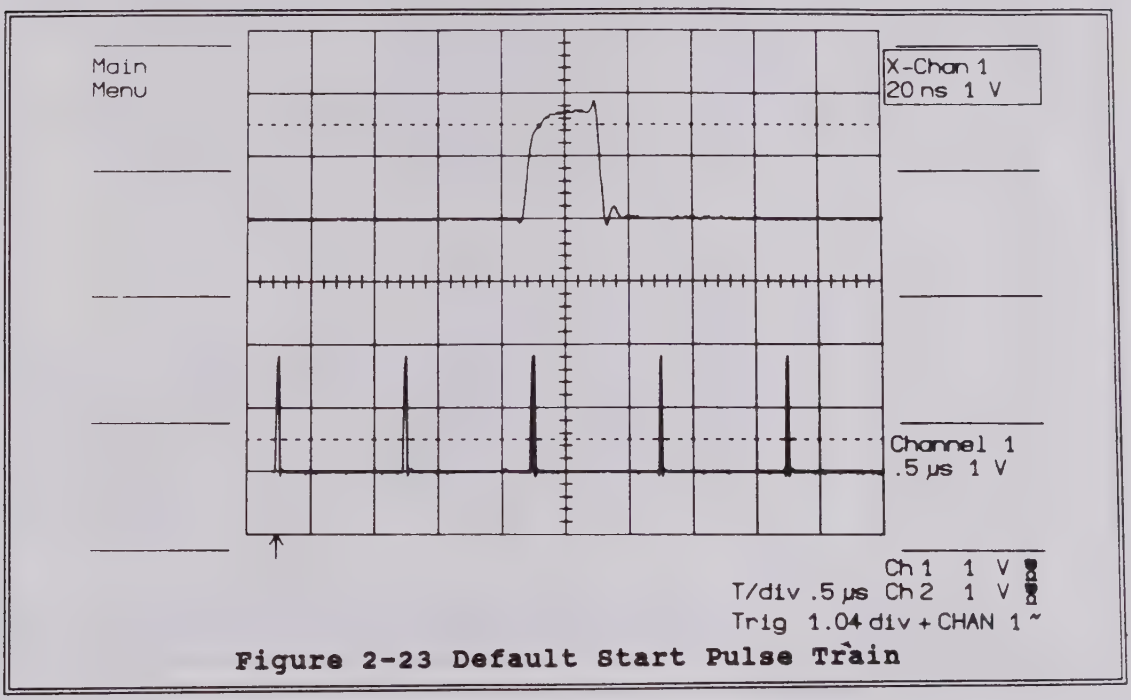


Figure 2-23 Default Start Pulse Train

ACTION

RESULT

SET OSCILLOSCOPE TO:
Channel 1: .5 V .5 μS 50 Ω dc
Channel 2: .5 V .5 μS 50 Ω dc
Trig: AC coupled Source: External
Slope: Positive

CONNECT: LeCroy 9100 START output to scope external trigger in; SYNC output to scope Channel 1; MARKER output to Channel 2.

Type: **ibwrt <Enter>**
"tmod rec,2;"<Enter>
Adjust scope trigger level.

Trigger mode changes to recurrent, with 2 repetitions. Each channel displays a series of 1.5 V pulses, ≈100 nS wide, and 2.1 μS apart (see Fig.2-24, next page).

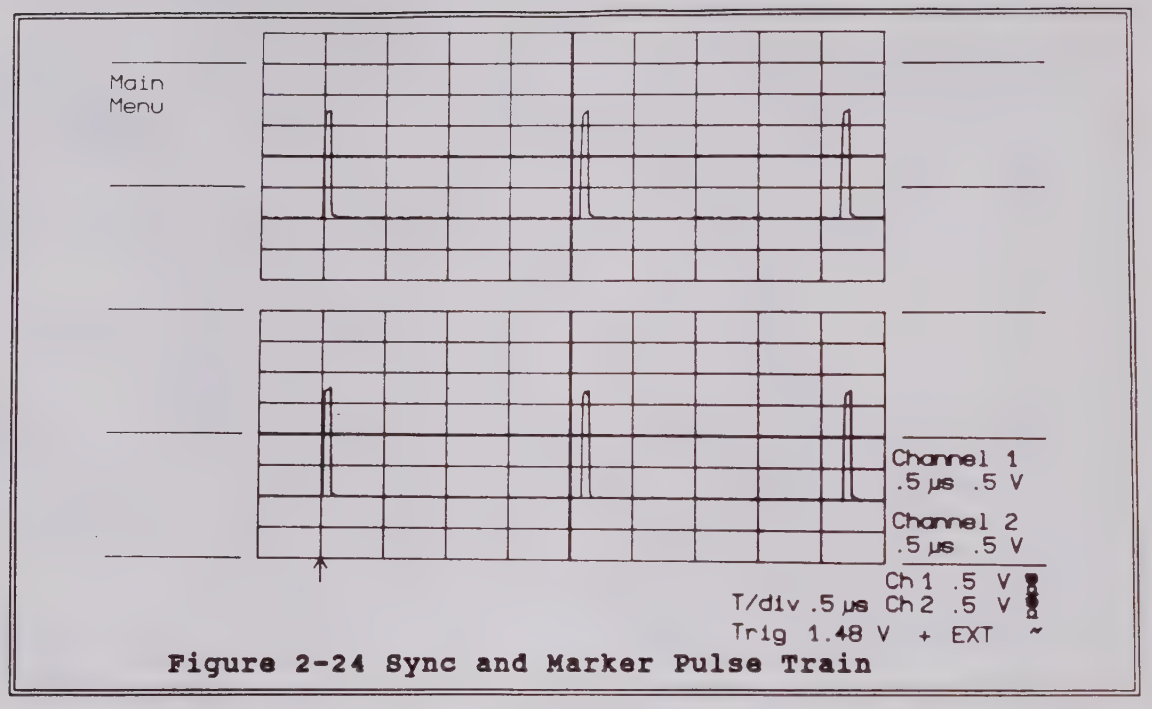


Figure 2-24 Sync and Marker Pulse Train

Waveform Outputs

ACTION	RESULT
Type: **ibwrt <Enter>** **"smod dual;"<Enter>** **ibwrt <Enter>"tmod con;"** **<Enter>**	Loads & runs a dual channel sinewave in continuous mode.
CONNECT: LeCroy 9100 CHAN 1 output to scope Channel 1; CHAN 2 output to scope Channel 2	Scope displays a pair of in phase sinewaves, 1 V p-p, with a 1 µsec period (see Figure 2-25).

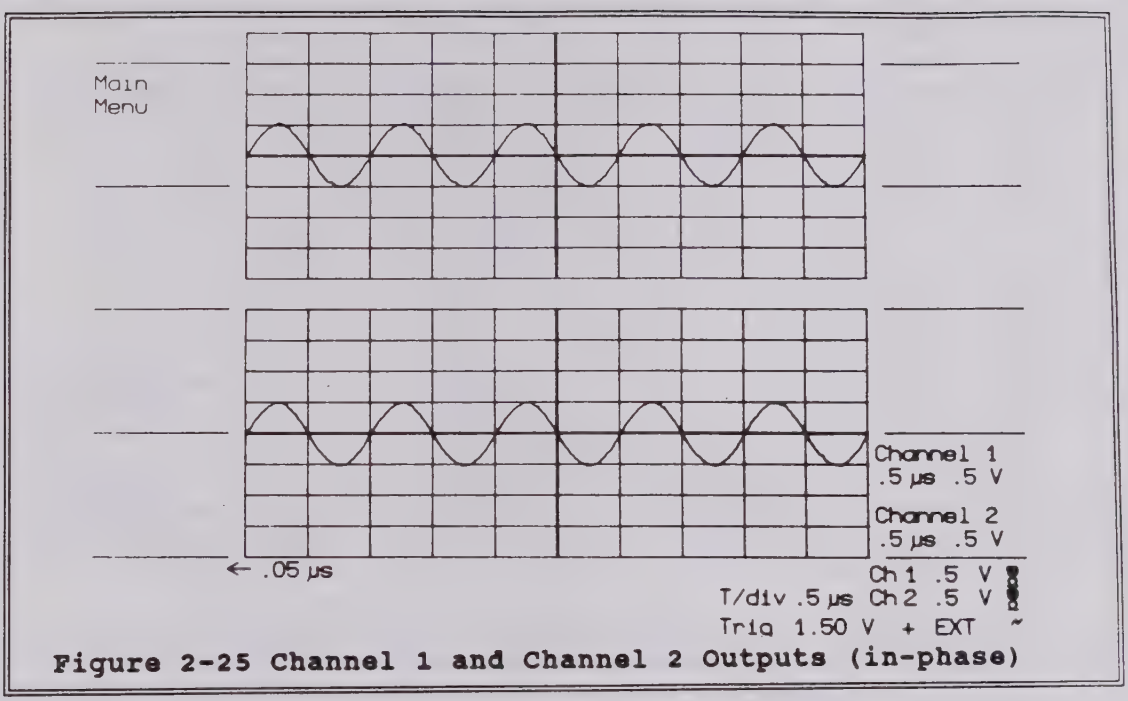


Figure 2-25 Channel 1 and Channel 2 Outputs (in-phase)

ACTION	RESULT
Type: **ibwrt <Enter> "sum on;" <Enter>**	WAVEFORM OUTPUTS sections CHAN 2 LED goes out and SUM 1+2 comes on. 9100 internally sums channels 1 and 2 to create a 2 V p-p sinewave (see Figure 2-26, next page).

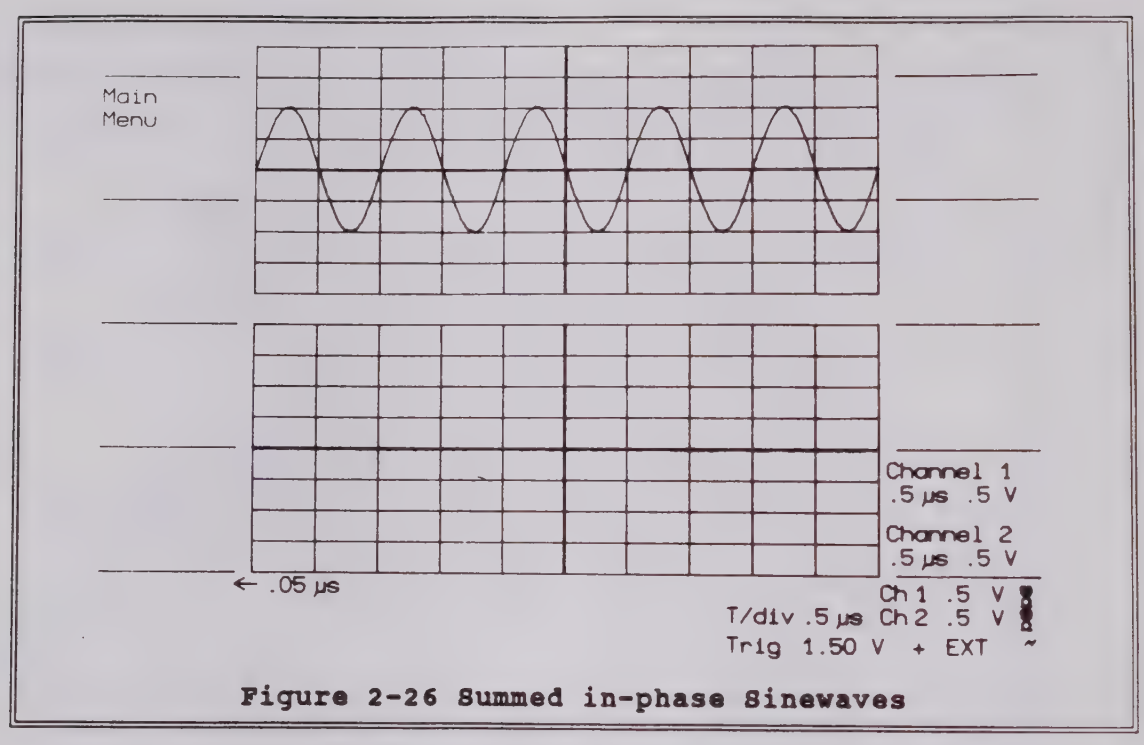


Figure 2-26 Summed in-phase Sinewaves

ACTION	RESULT
Type: **ibwrt <Enter> "sum off;" <Enter>**	CHAN 2 LED comes on. SUM 1+2 LED goes off. Waveform appears as in Figure 2-25.
DISCONNECT: CHAN 2 output from oscilloscope.	
CONNECT: CHAN 2 output to the INPUTS section SUM BNC.	
Type: **ibwrt <Enter> "xsum on;" <Enter>**	Waveform appears as in Figure 2-26.
DISCONNECT: CHAN 2 output from the SUM input.	
CONNECT: CHAN 2 output to scope Chan 2 Input.	Waveform appears as in Figure 2-25.

ACTION	RESULT
Type: **ibwrt <Enter> "xsum off;" <Enter> ibwrt <Enter> "c1i on;" <Enter>**	STATUS section CHAN 1 INVERT LED comes on, channel 1's output is 180° out of phase as in Figure 2-27.

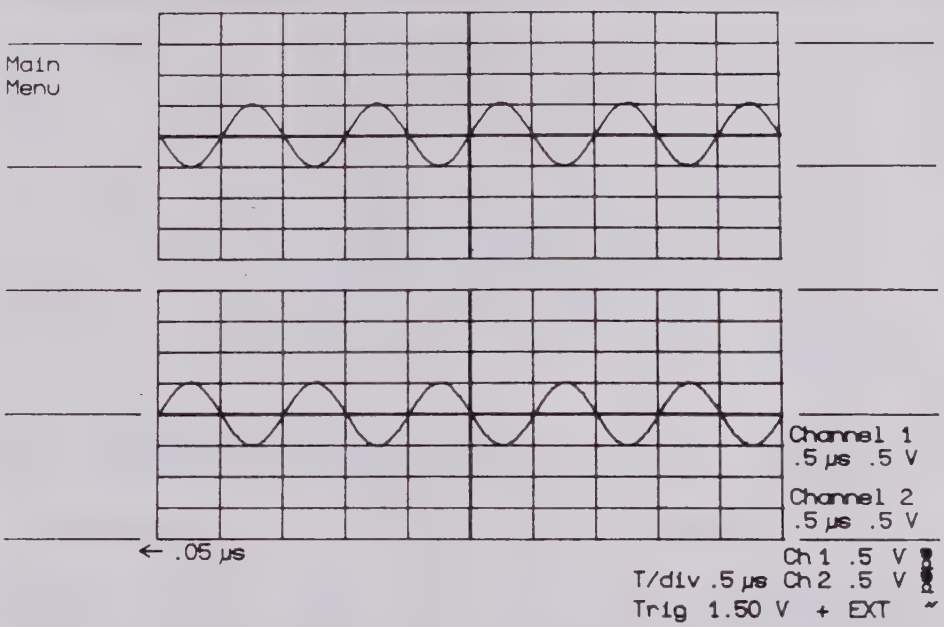


Figure 2-27 Channel 1 Inverted

Type: **ibwrt <Enter> "c1i off;" <Enter>**	CHAN 1 INVERT LED goes out. Sinewaves are in phase as in Figure 2-25.
Type: **ibwrt <Enter> "c2i on;" <Enter>**	CHAN 2 INVERT LED comes on, channel 2's output is 180° out of phase as in Figure 2-28.

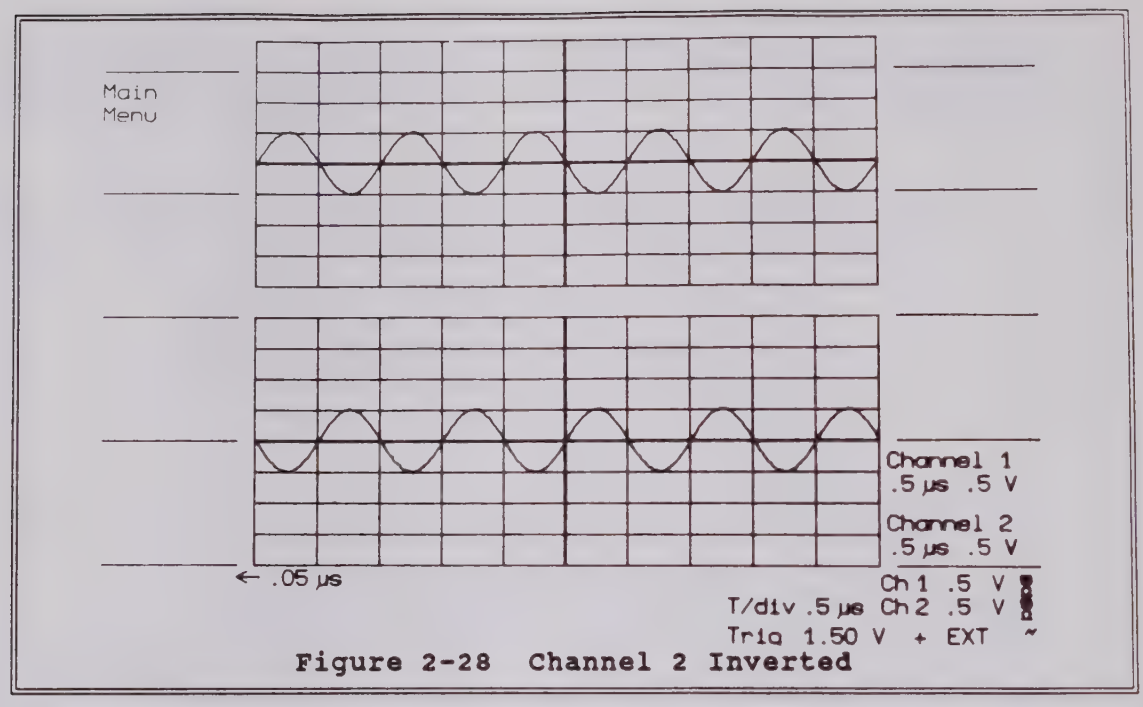


Figure 2-28 Channel 2 Inverted

ACTION	RESULT
Type: **ibwrt <Enter> "c2i off;" <Enter>**	CHAN 2 INVERT LED goes out, sinewaves are in phase as in Figure 2-25.
Type: **ibwrt <Enter> "tmod gate;" <Enter> ibwrt <Enter> "tlev 200mV;" <Enter>**	Changes trigger mode to gated, with a 200 mV threshhold level.
SET OSCILLOSCOPE TO: 1 µsec/div	
SET EXTERNAL SIGNAL SOURCE FOR: 500 kHz 1 V p-p sinewave.	
CONNECT: 9100 SYNC output to scope external trigger input.	
CONNECT: TRIGGER/GATE input to SIGNAL SOURCE output	STATUS section ARMED LED flashes on and off.
CONNECT: 9100 CHAN 1 output to scope channel 1	

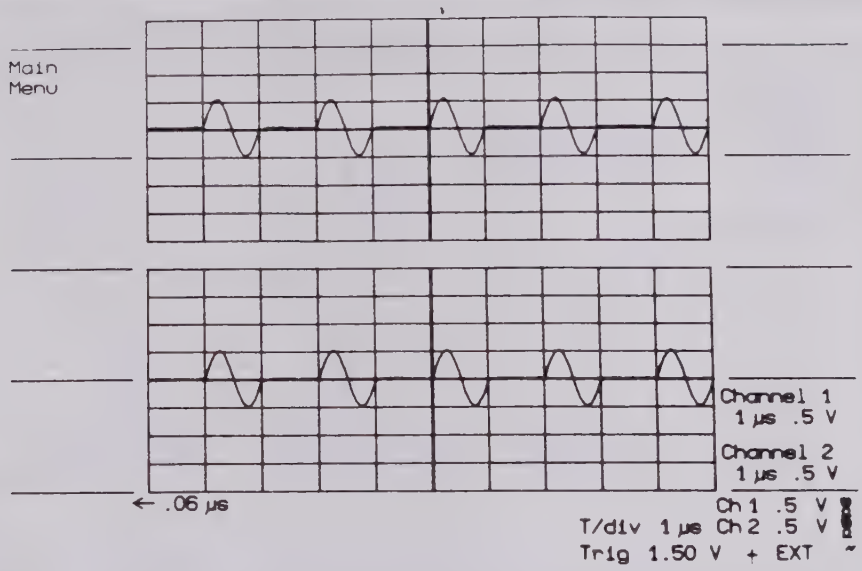


Figure 2-29 Externally Gated Dual Channel Signal Out

ACTION	RESULT
CONNECT: 9100 CHAN 2 output to scope channel 2	Scope displays a series of 1 µsec/cycle sinewaves, separated in time by 1 µsec as in Figure 2-29.
Type: **ibwrt <Enter>** **"tmod bur,3;" <Enter>** **ibwrt <Enter>** **"tsou ext,on;" <Enter>**	Bursts of 3 sinewaves appear, each burst separated in time from the previous by 1 µsec. as in Figure 2-30, next page. ARMED LED continues to flash.

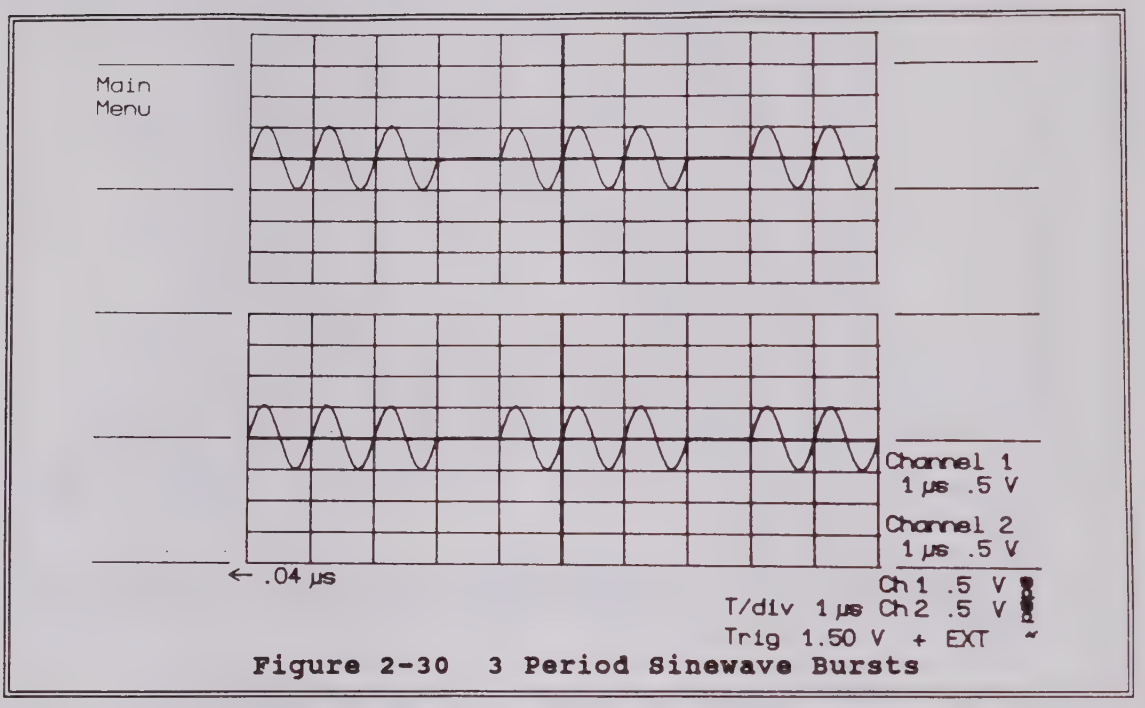


Figure 2-30 3 Period Sinewave Bursts

ACTION	RESULT
Type: **ibwrt <Enter> "tmod sing;" <Enter> ibwrt <Enter> "tsou ext,off;"**	Changes trigger mode to single. ARMED LED remains lit. Channel 1 output ceases.

DISCONNECT: The external signal from the TRIGGER/GATE BNC.

Type: **ibwrt <Enter> "comm_local;"** Return to Local **<Enter>**

ACTION	RESULT
SET OSCILLOSCOPE TO: Single-shot Storage mode	
Press: INPUTS section MANUAL button.	A single cycle of a sinewave 1 μS long occurs for each push of the MANUAL button. See Figure 2-31.

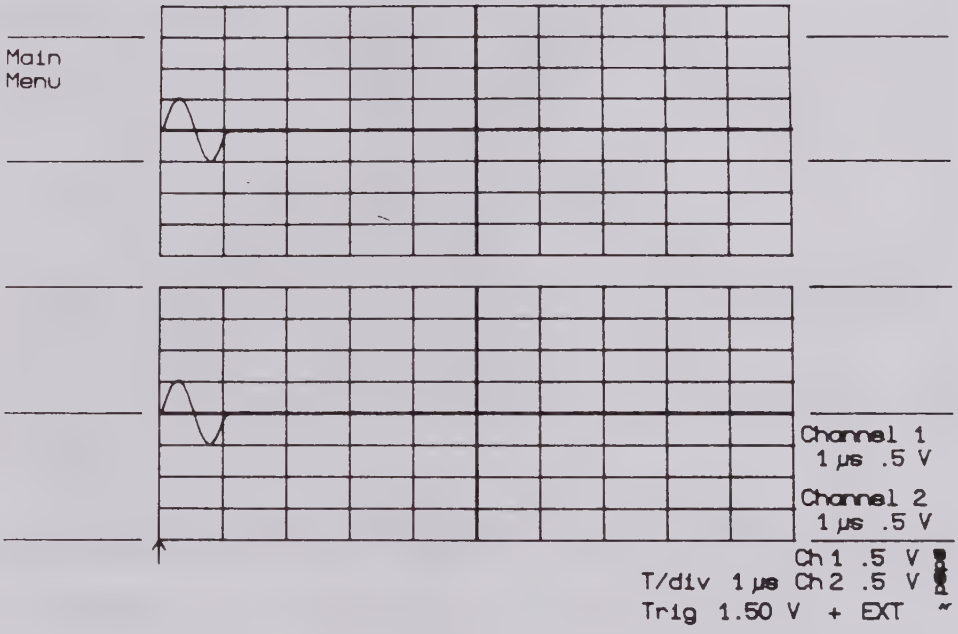


Figure 2-31 Single Trigger Mode

RAM Storage Battery Test

NOTE: Although the battery backed up storage should last for greater than two months, this test will fail if the battery has not been fully charged or the 9100 has not been used for an extended amount of time. In such cases it may be necessary to let the battery charge for approximately three hours before performing this test.

Type: **ibwrt <Enter> "comm_gpib;" <Enter> ibwrt <Enter> "c1a,2;" <Enter> ibwrt <Enter> "c2a,3;" <Enter> ibwrt <Enter> "tmod rec,3;" <Enter> ibwrt <Enter> "tdel,50;" <Enter> ibwrt**	Change Channel 1 amplitude to 2 V p-p, Channel 2 amplitude to 3 V p-p, and trigger mode to recurrent with 3 repetitions, and a trigger delay of 50 points. When started (by the 'go') the

"go;" ibwrt <Enter> "lset ibic.set;"	output should appear as in Figure 2-32. The remaining commands store the current AFG settings in the 9100's RAM-disk under the filename ibic.set.

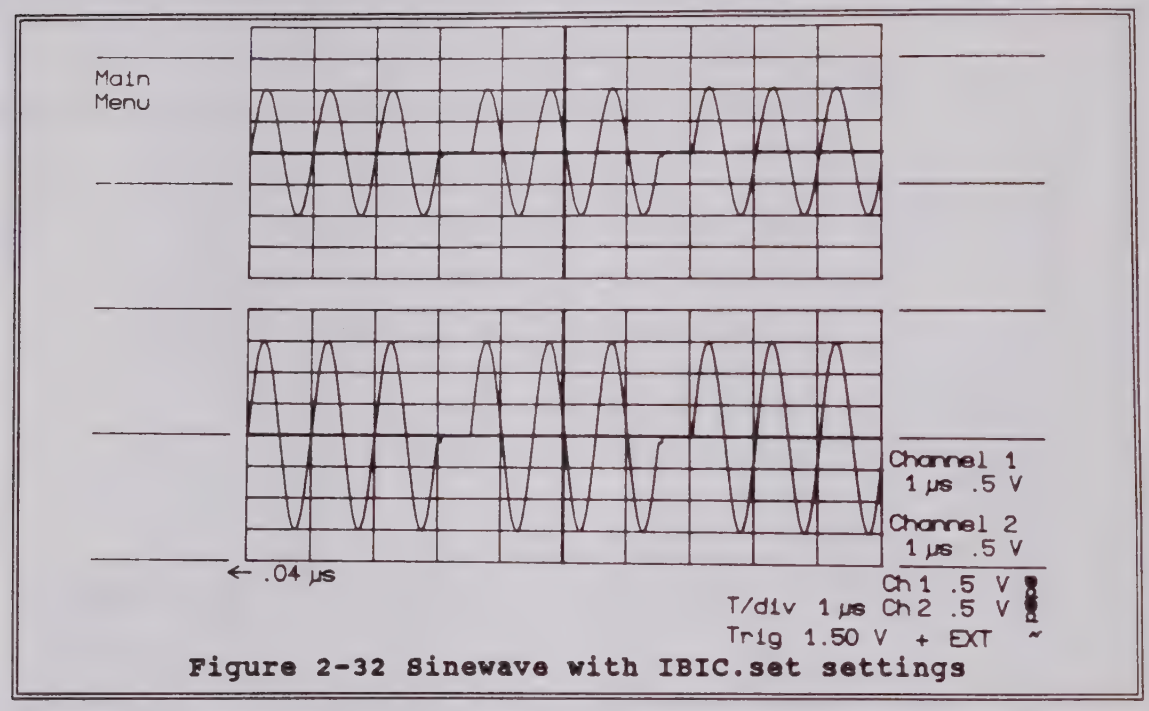


Figure 2-32 Sinewave with IBIC.set settings

ACTION	RESULT
After the Settings file has been learned, turn the 9100's power off for about 2 minutes.	
Re-apply power to 9100 & wait for LOCAL LED to light.	
Type: **ibwrt <Enter> "sine;" <Enter> ibwrt <Enter> "set ibic.set;" <Enter> ibwrt <Enter> "go;" <Enter>**	Waveform appears as in Figure 2-32.

CHAPTER 3

VERIFICATION OF ANALOG SPECIFICATIONS

3.0 Introduction

The following procedure will be used to verify the 9100's major analog specifications. The performance of the 9100 can be certified according to MIL STD 45662 using this procedure if the instruments used have been calibrated with NBS traceability.

3.1 Equipment Required

Analog Oscilloscope:	Dual Trace, 350 MHz,e.g.,Tektronix 485*
Digital Voltmeter:	5 or more digits, e.g. HP3468A
Frequency Counter:	7 or more digits, e.g. Philips 6672
Function Generator:	e.g., Tektronix FG504
Pulse Generator:	e.g., Tektronix PG502
Terminator:	50 Ω, 0.1%

*Note: *The overshoot and ringing characteristics of the front end of the oscilloscope to be used should be measured and recorded for future reference at some time prior to the testing of 9100s for overshoot and ringing.*

Before performing the tests that follow, the 9100 should be allowed to warm up for about 30 minutes, and a self-test should be executed.

3.2 Test Procedures

I. DC ACCURACY - ±1% or ±20 mV, whichever is greater.

Using the 9100/CP, program the AFG for a standard square wave, dual channel, at a frequency of 0.05 Hz. Set both channels for an offset of 0 mV, and Zref of 127.5. Connect the Channel 1 output of the 9100 to the DVM, terminated with the 0.1% 50 Ω terminator. Set the channel 1 amplitude to each of the values listed in Table 3-1 above, and see that the positive and negative output levels fall within the prescribed limits. Repeat for the channel 2 output. If this test fails, the 9100-2 should be returned to the factory for service.

peak-to-peak amplitude	positive level min	positive level nom	positive level max	negative level min	negative level nom	negative level max
5 mV	-17.5 mV	+2.5 mV	+22.5 mV	-22.5 mV	-2.5 mV	+17.5 mV
10 mV	-15.0 mV	+5.0 mV	+25.0 mV	-25.0 mV	-5.0 mV	+15.0 mV
30 mV	-5.0 mV	+15.0 mV	+35.0 mV	-35.0 mV	-15.0 mV	+5.0 mV
75 mV	+17.5mV	+37.5 mV	+57.5 mV	-57.5 mV	-37.5 mV	-17.5 mV
150 mV	+55.0mV	+75.0 mV	+95.0 mV	-95.0 mV	-75.0 mV	-55.0 mV
300 mV	+130.0 mV	+150.0mV	+170.0 mV	-170.0 mV	-150.0 mV	-130.0 mV
500 mV	+230.0 mV	+250.0 mV	+270.0 mV	-270.0 mV	-250.0 mV	-230.0 mV
1 V	+480.0 mV	+500.0 mV	+520.0 mV	-520.0 mV	-500.0 mV	-480.0 mV
2 V	+980.0 mV	+1.0 V	+1.02 V	-1.02 V	-1.0 V	-980.0 mV
3 V	+1.48 V	+1.5 V	+1.52 V	-1.52 V	-1.5 V	-1.48 V
7 V	+3.465 V	+3.5 V	+3.535 V	-3.535V	-3.5 V	-3.465V
10 V	+4.95 V	+5.0 V	+5.05 V	-5.05 V	-5.0 V	-4.95 V

Table 3-1 : DC Accuracy Test Limits

Note: The 3 tests below can be all be performed at the same time, since they all require the same set-up.

II. TRANSITION TIMES - ≤5 nsec

Using the 9100/CP, program the AFG for a dual channel standard square wave, and set the amplitude for both channels to 10 V (offset of both channels should be 0, Zref should be 127.5, and filters must be off). Set the square wave frequency to 1 MHz. Connect the AFG's channel 1 & 2 outputs to the oscilloscope's channel 1 & 2 inputs, and trigger the oscilloscope on the rising edge of the signal on channel 1. Measure the risetimes of the AFG's outputs. Both channels should have risetimes of 5 nsec or less. Reset the oscilloscope to trigger on the falling edge of the signal on channel 1, and measure the falltimes of both AFG outputs. Falltimes should also be 5 nsec or less. Reset the amplitude of both AFG channels to 1 V and repeat the above measurements. Again all transition times should be 5 nsec or less.

III. OVER/UNDERSHOOT AND RINGING - ≤5% of peak-to-peak amplitude

Note: The over/undershoot and ringing characteristics of the front end of the oscilloscope to be used should be measured and recorded for future reference at some time prior to the testing of 9100s for over/undershoot and ringing.

Using the 9100/CP, program the AFG for a dual channel standard square wave, and set the amplitude for both channels to 10 V (offset of both channels should be 0, Zref should be 127.5, and filters must be off). Set the square wave frequency to 1 MHz. Connect the AFG's channel 1 & 2 outputs to the oscilloscope's channel 1 & 2 inputs, and trigger the oscilloscope on the rising edge of the signal on channel 1. Set the oscilloscope for a vertical scale of 500 mV/div., and measure the overshoot and ringing of the positive transitions on both AFG channels.

Subtract the overshoot of the oscilloscope's front end from this measurement. The results should be 500 mV or less for both channels. Reset the oscilloscope to trigger on the falling edge of the signal on channel 1 and measure the undershoot and ringing on both AFG channels, again subtracting the oscilloscope's undershoot. Once again, the results should be 500 mV or less for both channels. Reset the amplitude of both AFG channels to 1 V and repeat the above measurements with the oscilloscope's vertical scale at 50 mV. The results should now all be 50 mV or less.

IV. PHASE DIFFERENCE BETWEEN CHANNELS - ≤1 nsec

Note: The connecting cables between the 2 AFG outputs and the 2 oscilloscope inputs MUST *be of equal length for this test.*

Using the 9100/CP, program the AFG for a dual channel standard square wave, and set the amplitude for both channels to 200 mV (offset of both channels should be 0, Zref should be 127.5, and filters must be off). Set the square wave frequency to 1 MHz. Connect the AFG's channel 1 & 2 outputs to the oscilloscope's channel 1 & 2 inputs, and trigger the oscilloscope on the rising edge of the signal on channel 1. Measure the time difference between the rising edges of the 2 AFG output signals at the 50% amplitude level. The difference should be 1 nsec or less. Reset the oscilloscope to trigger on the falling edge of the signal on channel 1, and repeat the delay measurement on the falling edges of the 2 AFG output signals. Again, the difference should be 1 nsec or less.

Note: If any of the 3 above tests fail, the 9100-2 board should be returned to the factory for service.

V. TIMEBASE ACCURACY - ±0.035% worst case, 2 ppm at setpoints

Connect the 9100's rear panel clock 1 output to the high frequency input of the frequency counter. Using the 9100/CP, program the AFG for a single-channel standard square wave at a frequency of 90 MHz. The counter should display a frequency between 179.999640 MHz and 180.000360 MHz. Change the square wave frequency to 71.25 MHz. The counter should then display a frequency between 142.499715 MHz and 142.500285 MHz. Next, change the square wave frequency to 56.25 MHz. The counter should then display a frequency between 112.499775 MHz and 112.500225 MHz.

If any of the above measurements is not within the specified limits, the following adjustment may be made. First, power down the 9100, remove the top cover and drop the front panel. Next, remove all ribbon and coaxial cables connected to the three top boards in the system (the 9100-2, -1, and -6 cards, from the top down), and then remove those 3 cards. Replace these cards such

that the -2 resides in the lowest available slot, the -1 is 2 slots above that (in the 2nd slot from the top), and the 9100-6 card is on the top. Re-connect the coax cables numbered 8 and 9 to J608 and J609, respectively, on the -6 card. Restore power to the 9100, and set it for a clock rate of 200 MHz. The trim cap at the rear, right hand side of the -6 card (directly adjacent to the 4 MHz crystal) should then be adjusted for a reading on the frequency counter as near to 200.000000 MHz as is humanly possible. If this adjustment cannot be made such that the frequency counter reading is stable to within ±1 least significant digit on a 7 digit counter, replace the -6 card and repeat this test from the top. Remember to restore the cards to their original positions and re-connect all cables before replacing the front panel and top cover.

VI. ADDITIONAL TESTS

The following tests are included for completeness. They test internal adjustments which do not have data sheet specifications. They may be considered optional.

Clock Input Threshold - Range: ±2.5 V, Resolution: 20 mV.

Range Test - Using the 9100/CP, load the dual channel arbitrary waveform A.wad, change the AFG's Clock Source to External, and the Clock Level to +2.5 V. Drive the 9100's rear panel Ext. Clock input with a 0 to +3 V square wave at 20 MHz from the PG-502, and issue the GO command from the CP. The resulting waveform output should be an up-going ramp on both channels, with a 2.56 μS period. Decrease the amplitude of the external clock signal until threshold is reached, i.e. until the AFG's waveform output begins to distort. This should occur when the clock amplitude is between 2.48 and 2.52 V p-p. Repeat the above procedure with a 0 to -3 V clock signal and the Clock Level set at -2.5 V. Issue an abort command when finished.

Resolution Test - Set up the FG-504 for a 20 MHz Triangle wave, 500 mV p-p, centered at 0V (i.e. -250 mV to +250 mV). Examine this signal carefully on the oscilloscope and make whatever amplitude or frequency adjustments are necessary to make the slope of this signal 20 mV/nsec. Apply this signal to the 9100's rear panel Ext. Clock input. Set the Clock Level to -200 mV, and the Delta under the Clock Level menu to 20 mV. Trigger the oscilloscope on the trigger output of the function generator. Issue the GO command and observe the AFG's Clock 1 output (rear panel) on the oscilloscope, with a falling edge of the signal on the leftmost oscilloscope division at 1 nsec/box. Still in the Clock Level menu on the CP, press More (F3). The falling edge should shift 1 major division (±1 minor division) to the right. Press the F3 button a few more times, and see that each time threshold is increased by 20 mV, the clock edge in question moves

1 nsec to the right. Reset the Clock Level to +200 mV and relocate a falling edge of the Clock output on the rightmost oscilloscope division, and press Less (F4). The falling clock edge should now shift 1 major division (±1 minor division) to the left. Press F4 a few more times and check that the clock edge shifts 1 nsec to the left each time threshold is decreased by 20 mV.

If either of the above tests fail, an adjustment may be made on the 9100-6 card which may rectify the problem. Put the -6 card in the top position within the 9100 mainframe (see the second paragraph under the Timebase Accuracy heading for details on how this can be done). Look for the Rev. level on left-hand side of the board, near the front. If the Rev. is E or F, there is only one adjustment, for the gain in the threshold DAC circuit. If the Rev. is G or higher, there are adjustments for both gain and offset.

Some revision F boards are updated to revision G, this can be determined by the presence of the offset potentiometer.
If the 9100-6 card is Rev. E or F, the adjustment may be made as follows. Use the CP to set the Clock Level to -2.5 V, and measure the voltage at pin 7 of U12. Adjust potentiometer R132 for -1.25 V ±20 mV. Note the voltage after trimming, and use the CP to reset the Clock Level to +2.5 V. The voltage should change to about +1.25 V, probably a bit less. Re-trim R132, trying to balance out the difference such that the measured positive voltage is less positive than nominal by the same amount as the measured negative voltage was more negative than nominal. For example, suppose that, after trimming, the nominal -1.25 V measured -1.265 V, and the nominal +1.25 V measurement, before re-trimming, is +1.215. The negative measurement is then 15 mV more negative than nominal, while the positive measurement is 35 mV less positive. The difference between these variations from nominal is 20 mV. Split this difference, and re-trim such that the positive measurement is +1.225 V (10 mV more positive than it was). Return the Clock Level to -2.5 V, and you should measure something very close to -1.275. Try to trim such that the variations in the difference from nominal are within ±10 mV.

If the 9100-6 is Rev. G or higher, follow this adjustment procedure. First, use the CP to set the Clock Level to 0 V. Measure the DC voltage at pin 7 of U12, and adjust potentiometer R68 for 5 mV ±0.5 mV. Next, set the Clock Level to +2.5 and adjust potentiometer R132 for a DC reading of +1.25 V ±5 mV. Finally, set the Clock Level to -2.5 V. The DC voltage at pin 7 of U12 should now be within 10 mV of -1.25 V.

If the adjustments above cannot be made to within the specified limits, or if the problem still exists after the above procedure is completed, the 9100-6 should be returned to the factory for service.

Trigger Input Threshold - Range: ±2.5 V, Resolution: 20 mV.

Range Test - With the dual channel arbitrary waveform A.WAD still in memory, change the AFG's Trigger Mode to Single, enable the front panel Trigger/Gate input (i.e. turn Trigger Source External on) and set the Trigger Level to +2.5 V. Drive the 9100's front panel Trigger/Gate input with a 0 to +3 V square wave at 200 kHz from the PG-502, and issue the GO command from the CP. The resulting waveform output should be an up-going ramp on both channels, with a 2.56 µsec period, and 2.44 µsec dead time between ramps. Decrease the amplitude of the external clock signal until threshold is reached, i.e. until the AFG's waveform output begins to disappear. This should occur when the trigger amplitude is between 2.48 and 2.52 V p-p. Repeat the above procedure with a 0 to -3 V trigger signal and the Trigger Level set at -2.5 V. Issue an abort command when finished.

Resolution Test - Set up the FG-504 for a 200 kHz Triangle wave, 500 mV p-p, centered at 0 V (i.e., -250 mV to +250 mV). Examine this signal carefully on the oscilloscope and make whatever amplitude or frequency adjustments are necessary to make the slope of this signal 20 mV/100 nsec. Apply this signal to the 9100's front panel Trigger/ Gate input. Set the Trigger Level to -200 mV, and the Delta under the Trigger Level menu to 20 mV. Trigger the oscilloscope on the FG-504's trigger output. Issue the GO command and observe the AFG's channel 1 output on the oscilloscope, using the delayed sweep if necessary to place the falling edge of the ramp on the leftmost oscilloscope division at 100 nsec/box. Still in the Trigger Level menu on the CP, press More (F3). The ramp's falling edge should shift 1 major division (±1 minor division) to the right. This should occur each time More is pressed, until the threshold is brought above the positive peak of the triangle wave.

If either of the above tests fail, an adjustment may be made on the 9100-6 card which may rectify the problem. Follow the adjustment procedure under the Clock Input Threshold heading above, making the gain adjustment at R43 instead of R132 for all cards, and the offset adjustment on cards of Rev. G or higher at R48 instead of R68. If the adjustments cannot be made to within the specified limits, or if the adjustment fails to remedy the problem, the 9100-6 should be returned to the factory for repair.

CHAPTER 4

DISASSEMBLY AND ASSEMBLY PROCEDURE

4.0 Introduction

The disassembly and assembly procedures detailed below refer to the exploded view of Figure 4-1. Please study this figure before attempting disassembly.

*********CAUTION*********

Before following disassembly procedure copy all internal waveform, setup and sequence files to a backup disk on the host computer. This can be done using the RECALL command, see the LeCroy 9100 Operator's Manual.

4.1 Removal of Connecting Cables and Covers

Disconnect the 9100 AFG from the AC power line. Remove all other interconnecting cables including the 9100/CP. The top and bottom covers are each secured by four M4 Pan Head screws (see Figure 4-1). Remove the screws using a 3/16" flat blade screwdriver. Remove the covers.

4.2 Removal of Front Panel

Place the unit on the feet of the back panel. The front panel is secured by four 4-40x3/4 screws (see Figure 4-1). Remove the screws using a #1 Phillips Head screwdriver. Carefully lay the 9100 AFG down (make sure surface is free of any debris) while holding onto loose front panel. Gently slide front panel out from the mainframe. The front panel is attached by several cables. To remove front panel completely, remove the following cables (see Figure 4-2).

Note: Extreme care must be taken whenever connecting or disconnecting any 9100 AFG cables. The grey ribbon cables eject automatically when the retaining ears are pressed outward. The SMB cables (single jacket white coax cables with gold connectors) disconnect by grasping the gold connector and pulling straight out. NEVER PULL ON ANY CABLE or WIRING.

1. Remove cables marked #5, #6 and #7 from 9100-2 board.
2. Remove cables marked #1, #2, #3 and #4 from 9100-6 board.

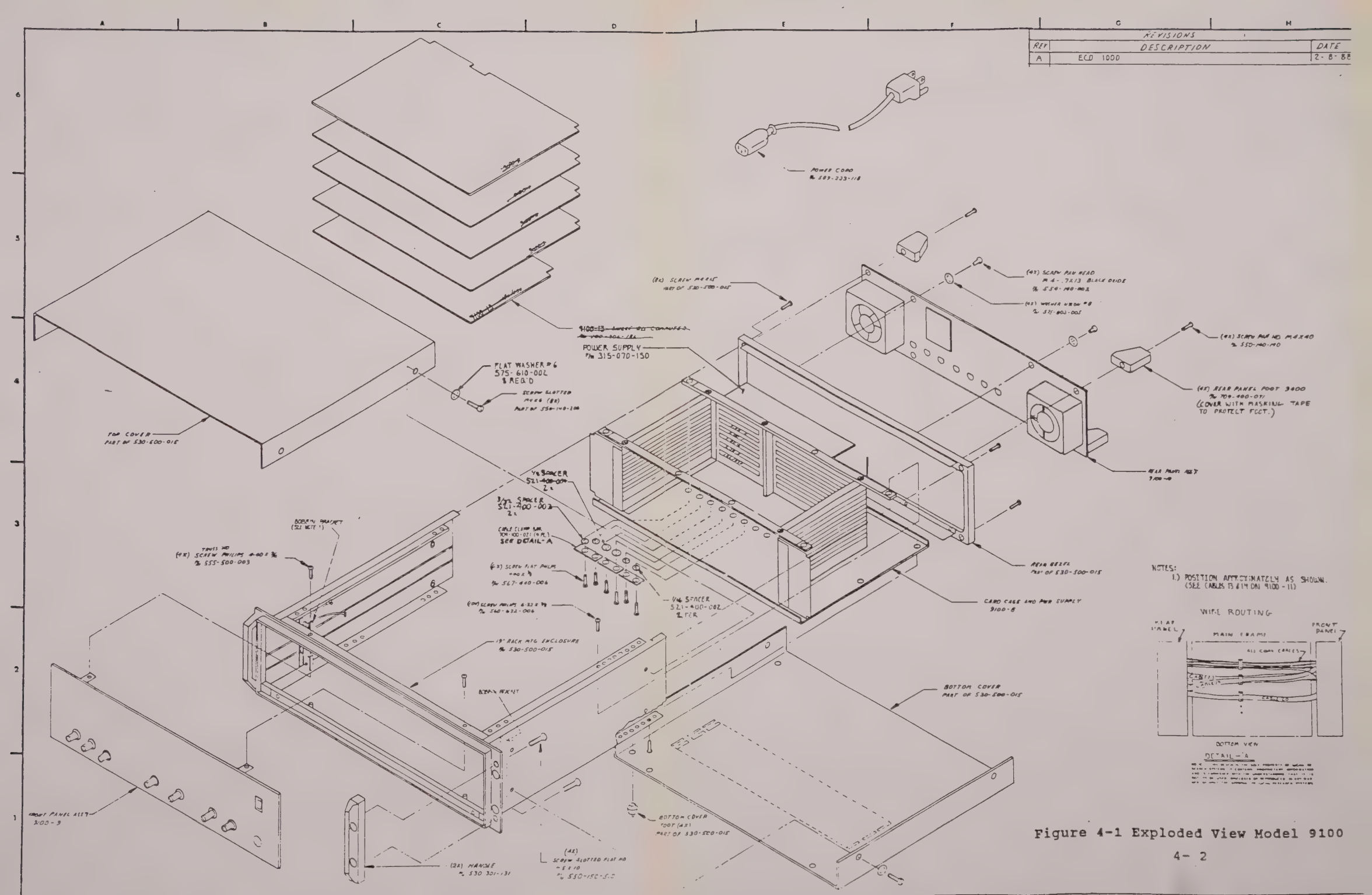
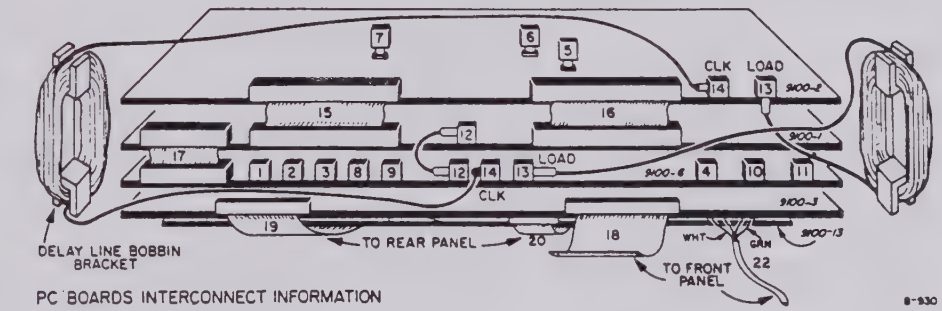
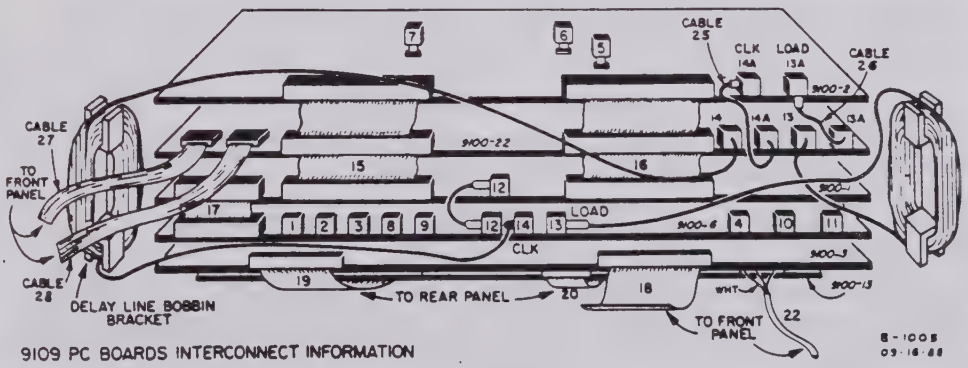


Figure 4-1 Exploded View Model 9100



PC BOARDS INTERCONNECT INFORMATION



9109 PC BOARDS INTERCONNECT INFORMATION

Figure 4-2 Board/Cable Interconnect

3. Remove gray ribbon cable marked #18 from 9100-3 board.
4. Remove cable marked #22 from 9100-13 (186/03A) bottom board.
5. Remove A.C. wire harness (connector on mainframe).

The front panel is now free from main frame.

Note: If the unit is a 9100/20 or 9100R the front panel will only be attached by the A.C. wire harness and cables marked #18 and #22.

4.3 Removal of 9100 AFG Boards

4.3.1 Removal of 9100-2 Analog Output Board

The 9100-2 board is situated at the top of the AFG. To remove first loosen and retract the board retaining brackets on the front of the card cage (see Figure 4-2), then remove the following cables.

1. Remove front panel cables marked #5, #6, and #7 (if not already removed).

2. Remove the 34-pin ribbon cables marked #15 and #16 going from the 9100-2 board to the 9100-1 board.

3. Remove delay line cables marked #13 and #14 from 9100-2 board.

When all cables are removed, carefully slide the 9100-2 board out of card cage being sure not to damage any of the tall components by bumping the AFG housing.

4.3.2 Removal of 9100-1 High Speed Memory Board

The 9100-1 board is located just below the 9100-2 board. Having already removed the 9100-2 board and associated cables, remove the following cables from the 9100-1 board (see Figure 4-2).

1. Remove the cable marked #12 going from the 9100-1 board to the 9100-6 board.

2. Remove gray ribbon cable marked #17 going from the 9100-1 board to the 9100-6 board.

After these cables are removed, carefully slide the 9100-1 board out of the card cage using the same precautions as in the removal of the 9100-2 board.

4.3.3 Removal of 9100-6 Trigger and Timing Generator Board

The 9100-6 board is the third board down from the top located two slots below the 9100-1 board. Having removed the 9100-2 and

9100-1 boards, remove the co-axial cables marked #8, #9, #10, #11, #13 and #14 from the 9100-6 (see Figure 4-2).

When all cables are removed slide the 9100-6 board out of the card cage using same precautions as in removal of previous boards.

4.3.4 Removal of 9100-3 Static RAM/GPIB Interface Board

The 9100-3 board is situated just below the 9100-6 board. Having removed the front panel, 9100-2, 9100-1 and 9100-6, remove the multicolor ribbon cable marked #19 from the 9100-3 board. Then slide out and remove 9100-3 board from card cage using same precautions as previous boards (see Figure 4-2).

4.3.5 Removal of 9100-13 (186/03A) CPU Board

The 9100-13 is the bottom board in the AFG main frame. It is possible to remove just the 9100-13 board without removing any of the other boards as in the case of updating PROMS (see Procedure for Replacement of ROM Set, Section 4.6, below). To extract the 9100-13 board after removal of all other boards remove the following cables (see Figure 4-2).

1. Remove multicolor ribbon cable marked #20.
2. Remove gray ribbon cable marked #21.

After removal of these cables, slide the board out of card cage being sure that the loose cables coming from back panel do not obstruct removal.

4.4 Replacement of 9100 AFG Boards

This is a simple reversal of the removal procedure, requiring care in the placement of cables and the insertion of cards into the card cage. Special attention must be given when inserting the card edge connector of pc board into the card cage connector because some boards may be slightly warped.

4.5 Removal and Replacement of 9100 AFG Power Supply

The power supply of the 9100 AFG is situated directly behind the card cage connectors. It is mounted by four screws directly underneath accessible from the bottom of the mainframe. To remove power supply disconnect cables J1-J4 being sure to remember proper orientation for when power supply is replaced (Note that J3 is not keyed). With 9100 AFG placed on its side use a #2 Phillips Head screwdriver and remove the four mounting screws from the backside of power supply (be sure to hold power supply while removing these screws). Carefully remove power supply by pulling straight up from mainframe.

To replace the 9100 AFG power supply, simply reverse the above procedure.

4.6 Procedure for Replacement of ROM Set in the 9100-13

Equipment Required:

Replacement ROM set - U40, U41, U73, U74

3/16" flat bladed screwdriver

#1 Phillips Head screwdriver

Replacement Procedure

The following instructions are a detailed guide for the replacement of the ROM set in a Model 9100 Arbitrary Function Generator.

1. Backup all internal waveform, setup and sequence files. All these files will have to be reloaded to insure compatibility with the new firmware.

2. Disconnect the LeCroy Model 9100 from the AC power line.

3. Remove all other interconnecting cables.

4. Remove the screws holding the top and bottom dust covers using the 3/16" flat blade screwdriver. These are eight, M4 pan head screws on the sides of the unit. Remove the covers.

5. Place the unit on its side and remove 4 front panel retaining screws from the top and bottom front rails using the #1 Phillips Head screwdriver.

6. Gently displace the front panel toward the top of the unit.

7. Remove the gray ribbon cable (#18) running from the front panel to the 9100-3 RAM board connector J1. Remove the multicolor ribbon cable (#19) from connector J2. See Figure 4-2.

8. Remove the coaxial cables marked 8, 9, 10, and 11, by pulling the connector bodies straight off the receptacle on the 9100-6 timebase/trigger board.

9. On the bottom (lowest) board in the card cage, (9100-13 CPU board) remove the 4 wire cable (#22), the multicolor ribbon cable (#20), and the gray ribbon cable (#21).

10. Use the #1 Phillips screwdriver to loosen the screws, holding the board retaining brackets on the front of the

card cage. Retract the retaining brackets away from the boards.

11. Remove the bottom board (9100-13 CPU board).

12. Lay the CPU board on a flat surface with the multibus edge connectors toward you. See Figure 4.3.

13. Locate the ROM's at the IC locations - U40, U41, U73 and U74. See Figure 4-3 for 9100-13 PROM locations.

14. Carefully remove each IC and replace the similarly marked IC from the ROM upgrade set.

15. Verify that each IC is properly oriented, i.e., the location notch and pin 1 are pointed away from the multibus edge connector. Make sure that all IC pins are properly inserted into the socket.

16. Carefully replace the CPU board into the card edge.

17. Engage the board retaining brackets on the front of the card cage with notches on the front of the circuit boards. Tighten the retaining screws.

18. Replace the multicolor ribbon cable (#20) to J2 on the 9100-13 CPU.

19. Replace the gray ribbon cable (#21) to the J1 connector on the 9100-13 CPU board.

20. Replace the 4 wire cable (#22) to the J1 connector on the 9100-13 CPU board.

21. Replace the gray ribbon cable from the front panel (#18) to J1 on the 9100-3 RAM board.

22. Replace the multicolor ribbon cable (#19) to J2 on the 9100-3 RAM board.

23. Replace the coaxial cables on the 9100-6 timebase/trigger board. (See Figure 4-2).

    Cable 11 - J611
    Cable 10 - J610
    Cable 9 - J609
    Cable 8 - J608

24. Replace the front panel and insert the four retaining screws.

25. Replace the top and bottom covers.

26. This completes the installation procedure.

27. With the power off, depress and hold the self test and manual trigger push button switches. Turn the power switch to the "ON" position and then release the push button switches. This will clear all existing RAM waveform, setup and sequence files.

28. Reload desired files.

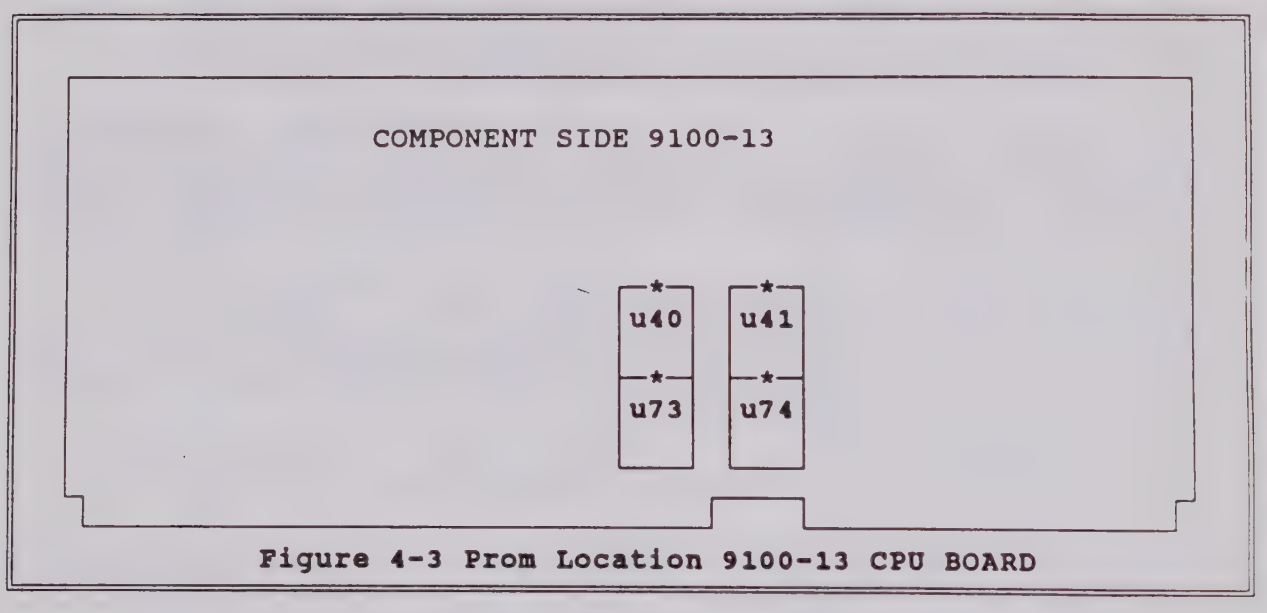


Figure 4-3 Prom Location 9100-13 CPU BOARD

CHAPTER 5

TECHNICAL CIRCUIT DESCRIPTION

5.0 Introduction

Technical Overview

Figure 5.1 illustrates the essential input/output connections, basic internal data flow and the internal organization of the 9100 Arbitrary Function Generator.

Input/Output Connections

These connections can be separated into three classes:

1 - Data and command inputs and status outputs from three sources;

- The General Purpose Interface Bus (GPIB) ... Refer to CHAPTER 8 for technical signal details of this interface. Operation of GPIB command interface is contained in Model 9100 Operator's Manual.

- The host serial interface, RS232 ... Refer to Model 9100 Operator's Manual for details of operation of RS232 command interface.

- The 9100 Control Panel ... Also detailed in Model 9100 Operator's Manual.

2 - Signal inputs and outputs which are of two types:

- Analog signal related, consisting of the two channel outputs(**CHAN 1, CHAN 2**), and the external sum input **SUM(CH1)**.

- The digital timebase and trigger signals consisting of four categories:

  - Timing reference signals, **SYNC, START, MARKER**
  - Time base clock outputs, **CLOCK1, CLOCK2**
  - Time clock outputs, **CLOCK1, CLOCK2**
  - External clock signal, **CLOCK IN - EXT**
  - External clock reference signal, **CLOCK IN - REF**
  - Trigger/Gate signal, **TRIG/GATE**

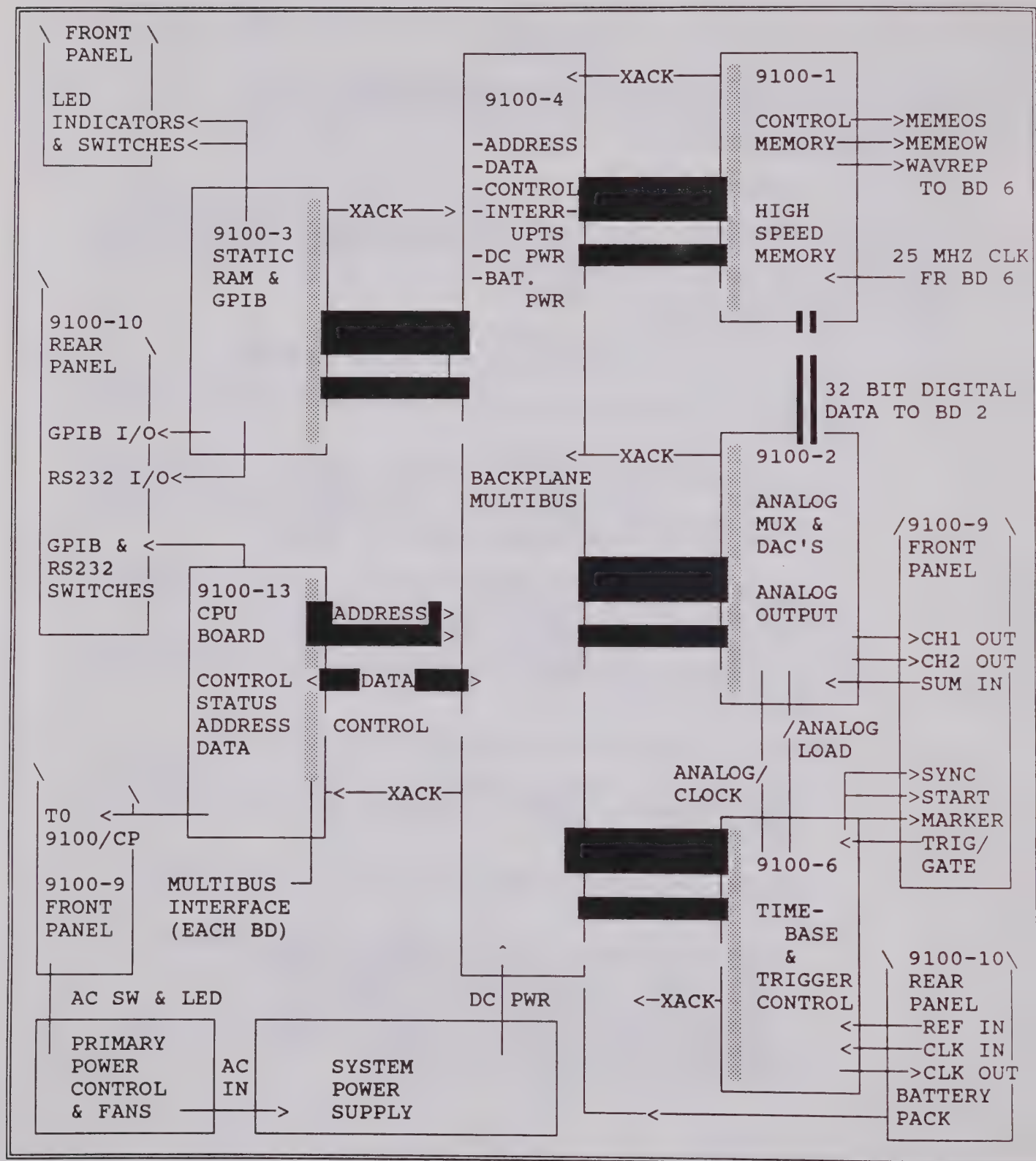


Figure 5.1 Board Level Block Diagram

3 - Power inputs which fall in two classes:

- Mains power which supplies the fans and the system dc power supply (part of 9100 - 8 Card cage & Power Supply)

- Battery backup source for the random access memory

Internal Data Flow

The 9100 AFG communicates with a host computer via either the GPIB or RS232 input/output connections. Commands and data received from the host are processed by the 9100-13 single board computer,stored in the 9100-3 static memory and executed by the combination of the 9100-1, 9100-2 and 9100-6. This latter combination of three boards functions as the actual signal generation core of the 9100 AFG. Structually the internal data flow closely matches the internal organization as discussed below.

Internal Organization

As illustrated, this organization consists of four distinct groups;

GROUP 1 - Waveform generation ...The 9100-1, 9100-2 and 9100-6 boards and their interconnections

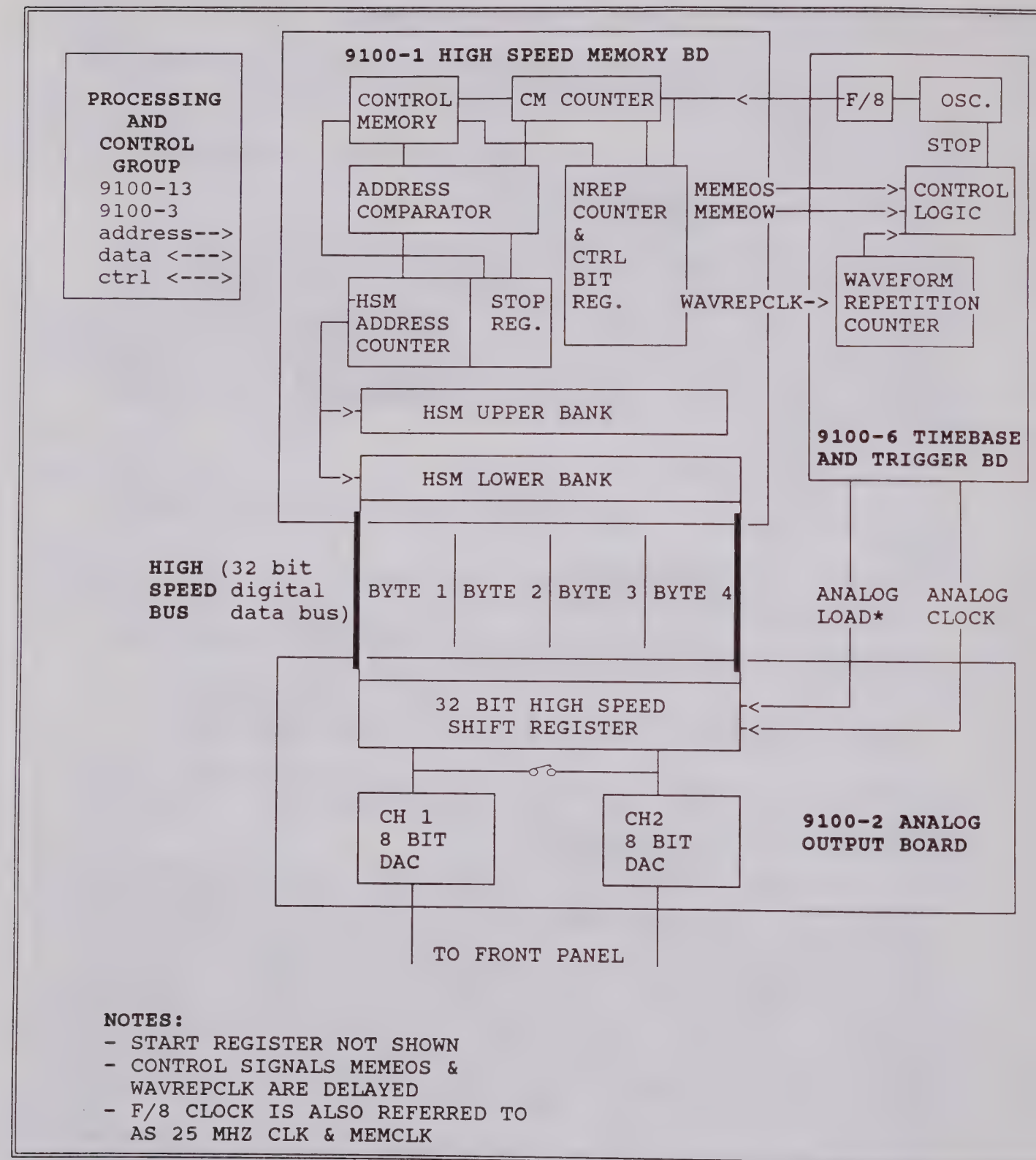
GROUP 2 - Processing and control ...The 9100-13 and 9100-3 boards and their interconnections

GROUP 3 - Status indication and external connection ...The 9100-9 and 9100-10 Front and Rear Panel subassemblies

GROUP 4 - Internal connection and power distribution ...The 9100-8 Card cage with power supply and 9100-4 backplane together with other internal cabling.

The intergroup communication between the first two groups is exclusively by the Multibus backplane as is dc power distribution. The Multibus backplane interface for each of the four non-cpu boards are similar, varying only in memory or port addresses and their decoding. An example interface is shown in the discussion of the 9100-1 (High Speed Memory Board)(see below). As that example shows, although there are 18 bus control signals controlled by the 9100-13 cpu-board, only seven are actually utilized by the other boards. The most important control signal is **XACK** which is returned by these boards to the 9100-13 to indicate that a data transfer has been completed.

The third group, status and connection, is represented physically by the 9100-9 and 9100-10, front and rear panels. As illustrated, all boards utilize the resources of these assemblies and are referred to below in each of the first two groups.



NOTES:
- START REGISTER NOT SHOWN
- CONTROL SIGNALS MEMEOS & WAVREPCLK ARE DELAYED
- F/8 CLOCK IS ALSO REFERRED TO AS 25 MHZ CLK & MEMCLK

Figure 5.2 Waveform Generation Group - Block Diagram

The fourth group, connection and power distribution, as mentioned, are also utilized by the first two groups and are discussed primarily in CHAPTER 6 - TROUBLESHOOTING.

Each of these groups is discussed below, including a description of the individual boards/subassemblies. Most descriptions refer to the block diagrams, however, where circuit details are described please refer to circuit schematics in APPENDIX B.

5.1 GROUP I - WAVEFORM GENERATION (The 9100-1, 9100-2 and 9100-6 Combination)

These three Multibus subassemblies perform as a subset of the Arbitrary Function Generator to hold a waveform in fast memory (9100-1), produce an analog output from that memory (9100-2), and generate the timebase/trigger (9100-6). The technical details of this group are discussed in the following subparagraphs to the functional block diagram level.

5.1.1 The 9100-1 High Speed Memory

General Description

The 9100-1 board basically consists of a block of High Speed Memory in which waveforms are stored and can be read out at high speed. The 9100-1 also contains a smaller memory called the control memory which controls the order in which the digitally stored waveform is read out. The board also contains a Multibus interface which allows the board to be programmed by a host computer. The purpose of this board is to read out a digitally stored waveform to the 9100-2 board which converts the digitally transferred data to become the analog points on the waveform. The speed at which the 9100-1 transfers its data to the 9100-2 board is controlled by a single clock input on the 9100-1 board (**25 MHz CLK** in Figures 5-1 and 5-2). This clock input is received from the 9100-6 time base board. The clock to the 9100-1 board is eight times slower than the actual running speed of the AFG. This is because the data is multiplexed and fed to the 9100-2 board four bytes at a time. Figure 5-2 shows the interaction within the Group I - Waveform Generation boards.

Definition of Waveform Terms

A waveform is a group of Data Segments stored in the High Speed Memory (HSM) to be read out of the board in the order determined by the data in the Control Memory (CM).

A segment is a continuous block of the High Speed Memory made up of any multiple of eight bytes. Its size can range from 72 bytes to the full 64K. A segment can be located in any chosen HSM location that is evenly divisible by eight. For special cases where a small waveform consisting of less than 72 points is needed the waveform must contain only one segment which is a

multiple of eight bytes in length and has a repetition count of one.

Each segment consists of eight bit data bytes which represent the digital values of the points in the waveform(i.e. values of 0 thru 255). Each segment of data in the HSM has a corresponding block of memory in the Control Memory which determines:

1) Where the particular Segment is to be fitted into the Waveform.

2) How many times the Segment will be repeated (up to 4095 times) before the next Segment of the Waveform begins.

3) Whether the Segment is the last Segment of the Waveform.

Any Segment in the HSM can be used more than once in different parts of the waveform. Each time a Segment is used, the control data for the Segments use, located in the Control Memory, contains a count which is programmed by the user to determine the number of times the Segment is to be repeated.

In order to repeat the entire Waveform a number of times (up to 65,535 times), the user specifies which Segment will be the last Segment of the Waveform. This is done by setting certain bits in the control block of the CM for that segment. The sequence goes back to the beginning after that Segment runs and a clock pulse is sent from the 9100-1 board to the 9100-6 board which updates a counter on the 9100-6 board which tells how many times the Waveform has been run.

A new segment entry is required in the control memory for each segment of the desired waveform and each segment must have at least one segment repetition count loaded in its control bit register. This waveform repetition counter on the 9100-6 board is programmed by the user with how many times the waveform is to be run and automatically stops the AFG when it receives the specified number of clocks from the 9100-1 Waveform that is running.

A waveform can be repeated a programmed number of times and may contain many Segments each of which can be used in more than one place in the Waveform and each of which can be repeated up to 4095 times each time it is used in the waveform.

For a one Segment waveform, the Segment repetition count can be loaded into the Waveform Repetition Counter on the 9100-6 board since either will repeat the waveform the desired number of times as long as the other is loaded with a count of one.

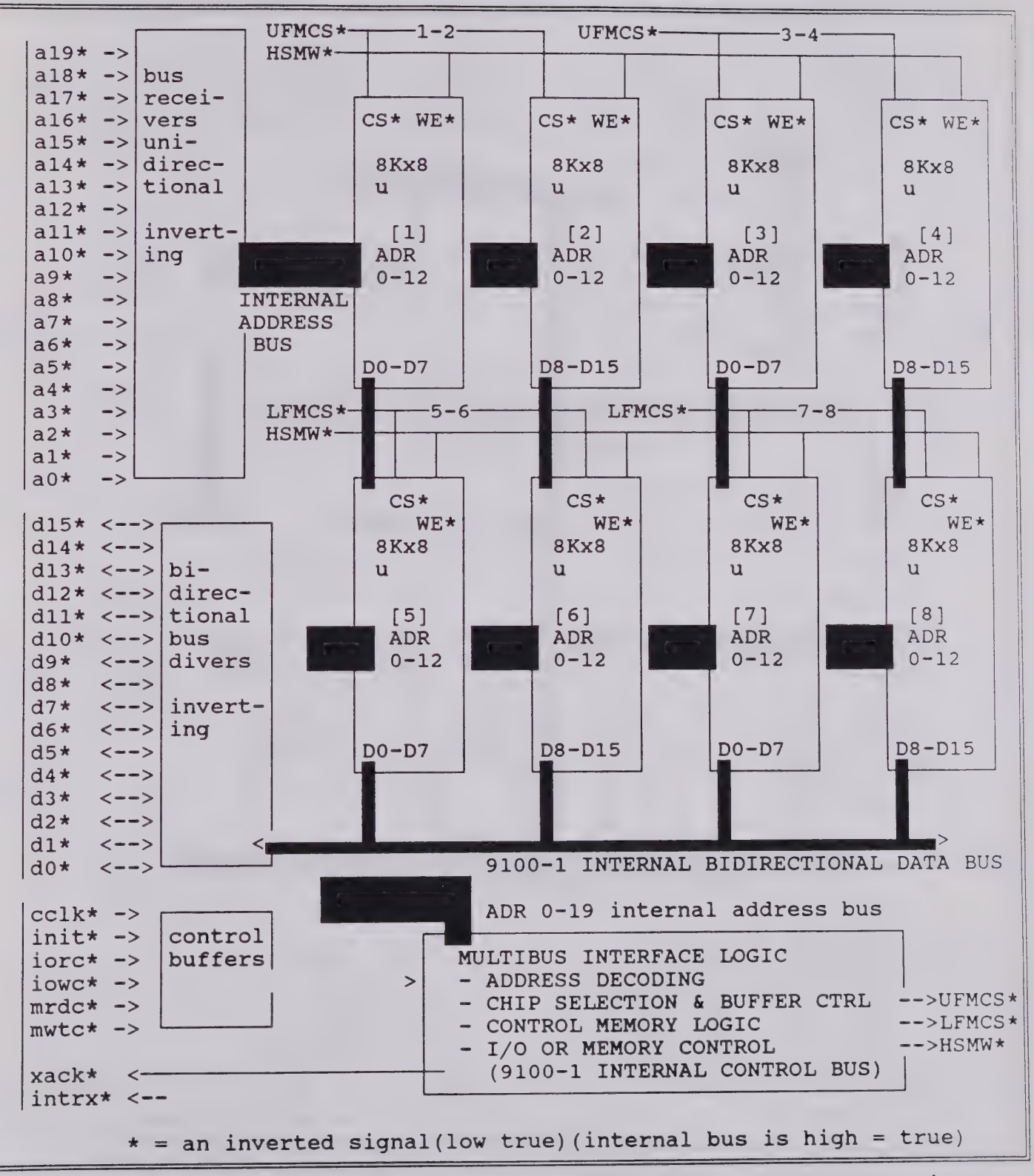


Figure 5.3 Dual Port High Speed Memory - Multibus Port(read/write)

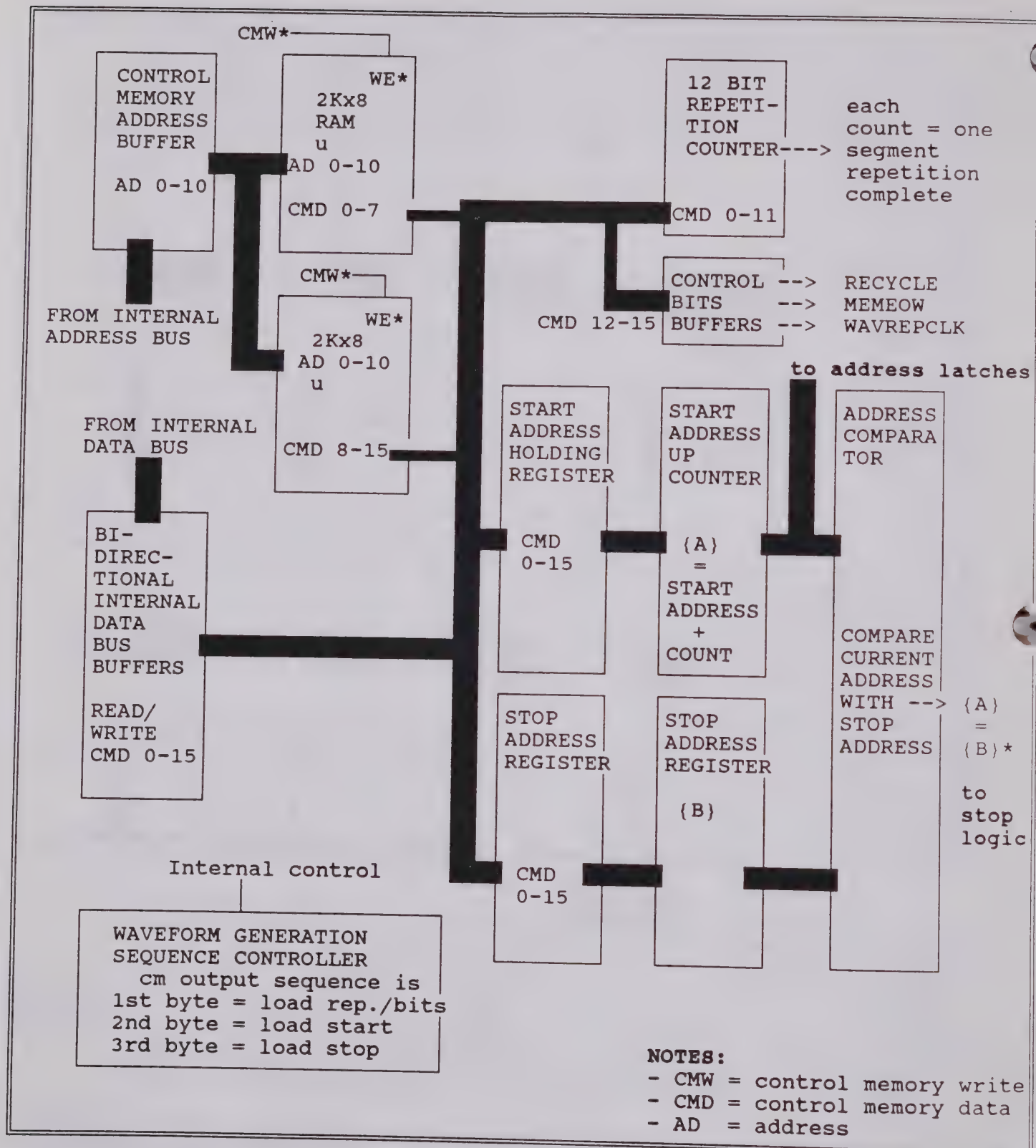


Figure 5.4 9100-1 Control Memory Functional Block Diagram

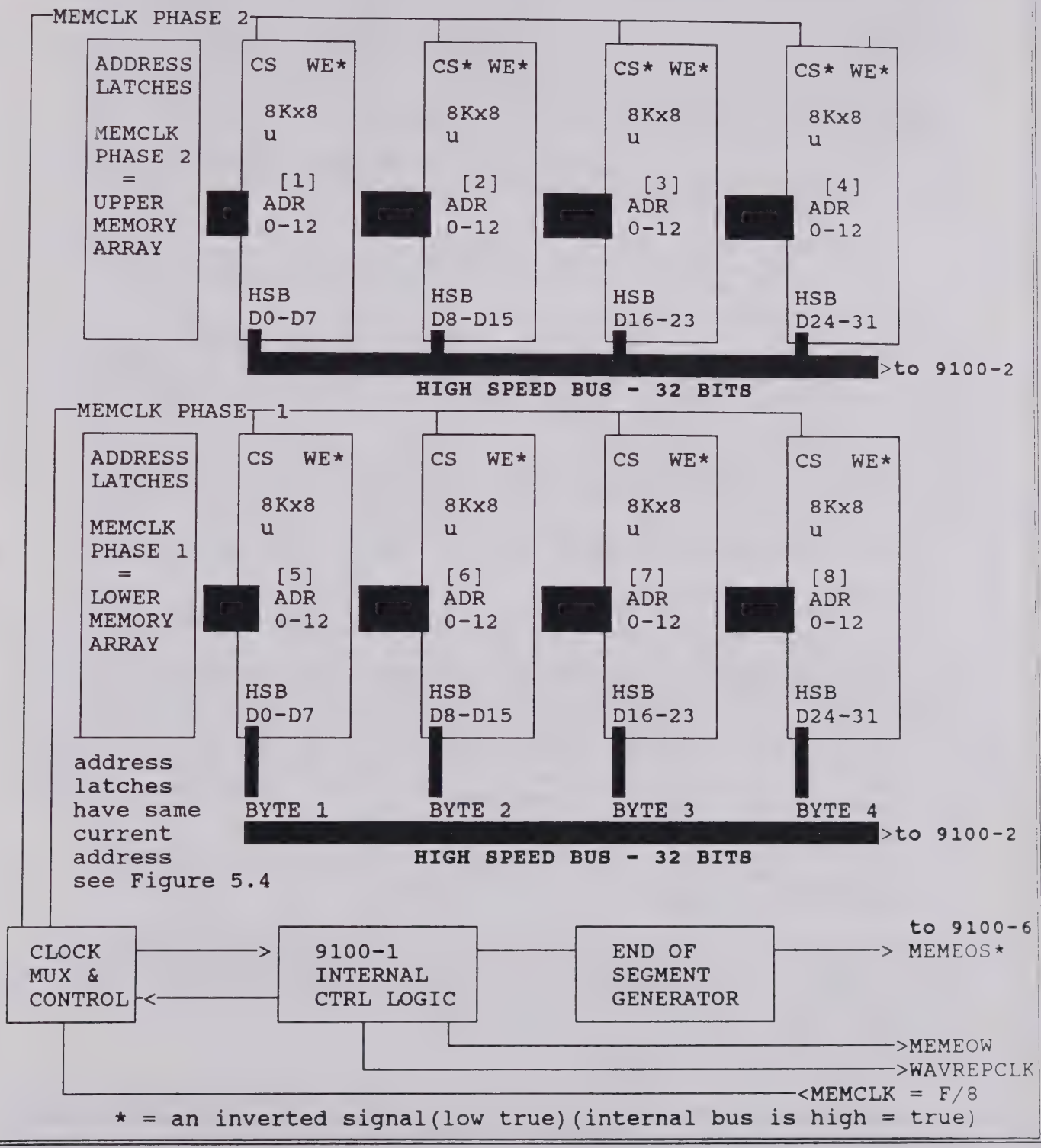


Figure 5.5 Dual Port High Speed Memory - High Speed Bus (read only)

Internal Functional Structure

Conceptually, the 9100-1 implements a dual port ram design, with the Multibus Port being a read/write port and the waveform generation port being a read only port. The control memory implementation is a similar dual port scheme. The basic function of the control memory is to provide sequence memory for the internal sequencer which actually controls the output of data to the 9100-2 during waveform generation. Internally the 9100-1 is organized into three functional structures

1) The Multibus interface to the High Speed Memory Array (See Figure 5-3, Dual Port High Speed Memory - Multibus Port)

2) The internal control logic and control memory structure, which includes the run-time(waveform generation) sequencer (See Figure 5-4, 9100-1 Control Memory Functional Block Diagram)

3) The Waveform Generation Port of the High Speed Memory to the 9100-2 Analog Board and the 9100-6 Timebase and Trigger Board. (See Figure 5-5, Dual Port High Speed Memory - 9100-2 Port)

The interface signals to the 9100-2 and the 9100-6 are discussed in their respective paragraphs, which follow.

5.1.2 The 9100-2 Analog Output Board

General Description

The 9100-2 takes the digital representation of the waveform being generated from the High Speed Memory (9100-1) and the clock signals from the clock generator and trigger processor (9100-6) and converts this information to analog form. The 9100-2 also contains circuitry to generate offsets, as well as to calibrate the 9100 under control of the 9100-13 CPU Board. The 9100-2 also contains a Multibus slave interface for communication with the instrument's CPU. There are no user adjustments on the 9100-2.

A simplified signal flow though the 9100-2 is illustrated in Figure 5.6 - Functional Block Diagram.

Each step in the signal flow will be described in detail below, as well as the calibration circuitry and the offset generation circuitry. The reader should note that the signal path is essentially identical for both output channels.

Digital Demultiplexer

Since the digital demultiplexing is done differently for single and dual channel modes of operation, they will be discussed separately in this section.

Dual Channel Mode

In dual channel mode, the digital representation of the two analog outputs is presented to the demultiplexer as a four byte wide word with each byte consisting of eight bits. In dual channel operation, bytes 0 and 1 contain the digital information for channel one and bytes 2 and 3 contain the digital information for channel two. At the maximum clock rate, one 32 bit word is clocked in every 20 nsec. This will give us a minimum of 10 nsec per point per waveform in dual channel mode. The clock input to the 9100-2 has a minimum period of 10 nsec during dual channel operation. A new 32-bit word is loaded into the demultiplexer by a 'load pulse'. One load pulse is received by the 9100-2 for every two clock pulses during dual channel operation.

Single Channel Mode

In single channel mode, the digital representation of the analog output is presented to the demultiplexer as a four byte wide word with each byte consisting of eight bits. In single channel operation, bytes 0, 1, 2 and 3 contain the digital information for channel one. At the maximum clock rate, one 32 bit word is clocked in every 20 nsec. This will give us a minimum of 5 nsec per point in single channel mode. The clock input to the 9100-2 has a minimum period of 5 nsec during single channel operation. A new 32-bit word is loaded into the demultiplexer by a 'load pulse'. One load pulse is received by the 9100-2 for every four clock pulses during single channel operation.

NOTE: The load, clock and data are all at ECL levels. ECL levels are defined as -.8 V true or high, -1.8 V low or false with -1.3 V being the threshold.

The load pulse is logically inverted, so high will be false. All the these signals come into the 9100-2 on the front of the board, so they are accessible for scoping purposes.

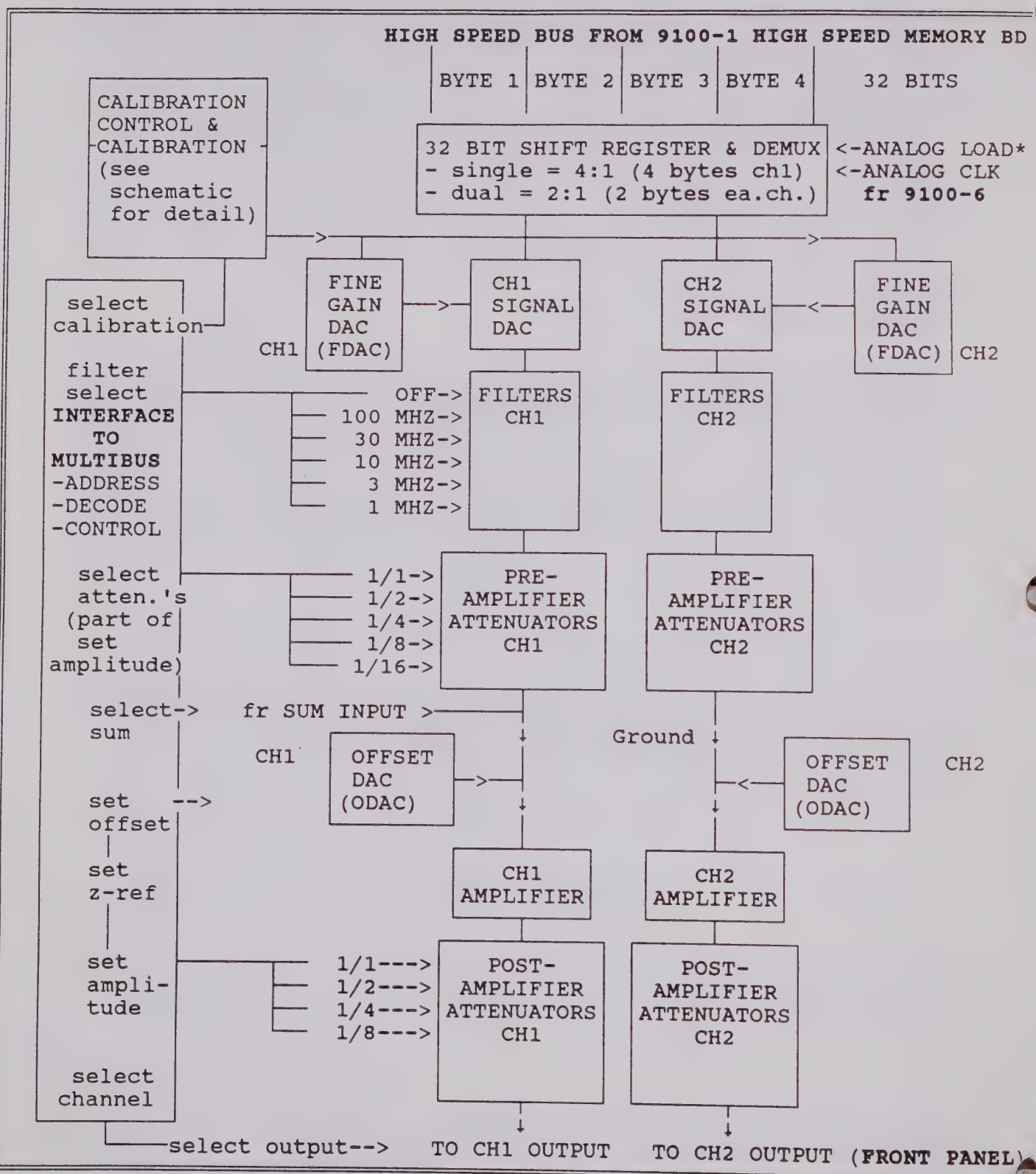


Figure 5.6 9100-2 Analog Output Bd - Functional Block Diagram

Each DAC also has a fine gain input, the function of which will be discussed below.

Signal Conditioning

As a signal is being clocked into the DAC, we will get a signal out of the DAC. The output of the DAC becomes more negative for larger input codes. Due to the characteristics of the output DACs used in the 9100, the signal still needs some conditioning before it is usable as an output signal. There are three stages of signal conditioning on the 9100-2. Each is described in detail below.

The first stage of signal conditioning for the output of the DAC is provided by a proprietary hybrid, developed by the LeCroy Corporation specifically for the 9100. This hybrid provides two types of signal conditioning, attenuation and filters, each under the control of the 9100's CPU. The hybrid provides the following attenuation ranges: divide by 1, divide by 2, divide by 4, divide by 8 and divide by 16. The filters are three pole Bessel filters that can be selected to operate at 1, 3, 10, 30 or 100 MHz or with filters off. This hybrid has an overall gain of 2/3. The hybrid also is connected to a compensating network so the high frequency response can be optimized at the factory.

When the 9100 is used with channels one and two being summed the output of the channel two attenuator and filter hybrid is summed with the output of the channel one attenuator and filter hybrid. The combined signal is fed to the inverting input of the channel one amplifier.

The output of the filter and attenuator hybrid goes through a 49.9 Ω resistor to the inverting input of a bipolar amplifier. The series resistor is in the circuit to match the 100 Ω output impedance of the hybrid to the 50 Ω input impedance of the amplifier. The non-inverting input for channel one is connected to ground via a resistive network when the external sum input is not being used. When the external sum input is being used, a different resistive network is used to terminate the input of the amplifier, and the external sum input is connected into the circuit through a resistive network and some protection diodes. The diodes limit the maximum voltage swing at the external sum input to plus and minus eight volts. If the protection diodes are made to conduct, the external sum input is automatically disconnected. The non-inverting input of the channel two amplifier is always connected to ground through a 51 Ω resistor.

The next stage of signal conditioning is another proprietary LeCroy hybrid. This hybrid provides another stage of attenuation. The various stages of attenuation are switched in and out by a system of relays. Attenuation ranges of divide by one, divide by two, divide by four and divide by eight are provided. Should a large voltage be accidentally connected to

the output, there is a circuit which will disconnect the output from the internal circuitry. It is not advised that the user test this feature. Also, a part of the output signal is tapped off the output signal for internal calibration purposes. the reader may recall that the 9100 will calibrate itself under internal computer control. During the calibration cycle, the outputs are not connected. The calibration cycle will be explained in greater detail below.

Offset Generation

There is an eight bit offset DAC for each channel. To write to the channel one offset DAC, one first will write the desired offset to address 0x800, and then write a strobe to 0x808. Similarly the offset DAC for channel two resides at address 0x840 with its strobe at 0x848. The output of the DAC is fed to a level shifting network and then summed into the inverting input of the channel's output amplifier. Channel two also contains a switching network so that when the 9100 is being used with channels one and two being summed, the offsets are also summed and the result is summed into the inverting input of the channel one output amplifier.

Calibration Circuit

The calibration circuit on the 9100-2 has inputs from Channel One output, Channel Two output, a voltage reference at +5 V, a 1/64 of 5 V voltage reference, a 0 V voltage reference and a temperature sensor. These inputs are switched by an input selection multiplexer and then fed to a very stable and predictable programmable gain amplifier. This signal, after amplification is fed to a twelve bit ADC (Analog to Digital Converter). When a calibration cycle is started, the input data from the input selection multiplexer is digitized. The data from this is used to calculate amplitude and offset corrections which are then used to compute the settings of the offset DACs and the fine gain DACs. The outputs of the fine gain DACs, after some conditioning, go to the Vref inputs of the channel one and channel two output amplifier. Thus there are no potentiometers of any significance on the 9100-2.

Adjustment Points

The technician may notice some adjustments on the 9100-2, and may attempt to change their setting to bring a malfunctioning unit back to satisfactory performance. This is not recommended. The only potentiometer that will have any effect on the calibration of the 9100-2 is the voltage reference potentiometer. Any other adjustments attempted will only be negated by the instruments own internal calibration cycle. If the 9100-2 fails to meet specification after a calibration cycle then the board is defective and cannot be fixed by recalibration. It is suggested that such boards be returned to the factory for exchange or repair.

5.1.3 The 9100-6 Timebase and Trigger Processing Card

General Description

The 9100-6 contains the timebase and trigger processing circuitry for the LeCroy Model 9100 Arbitrary Function Generator. It receives the trigger signal from some external source to commence waveform generation, provides for programmable delay from the receipt of the trigger to the start of the waveform, determines the rate of the waveform output in points per second, provides clocking signals to the fast memory (9100-1) and analog output (9100-2) boards, counts the number of waveform repetitions in burst mode, determines the exact point at which the waveform output stops, and provides the user with 4 timing outputs with which he can synchronize his measurement system.

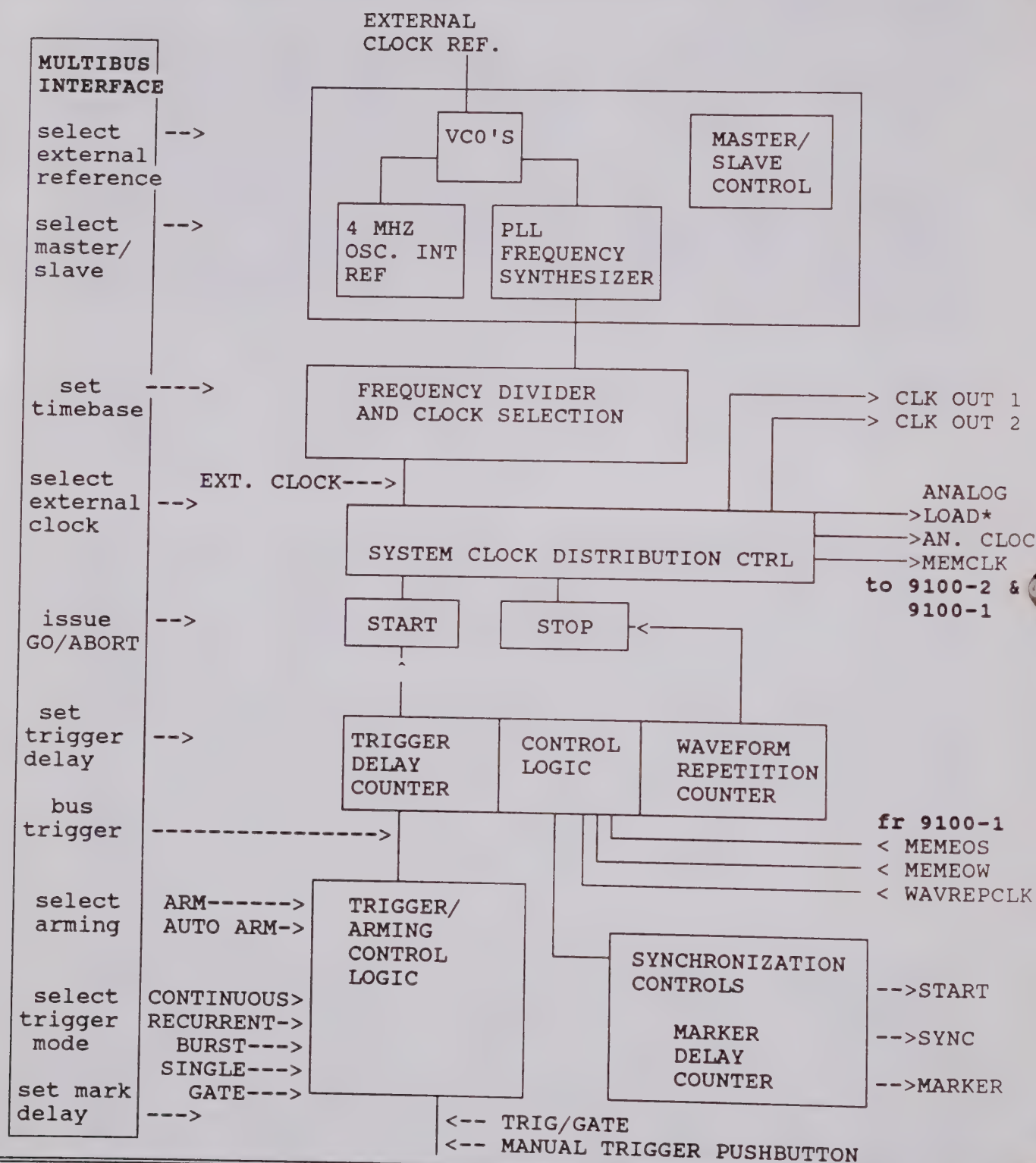


Figure 5.7 9100-6 Timebase/Trigger Bd.-Functional Block Diagram

Timebase

The internal timebase of the 9100-6 consists of 3 Voltage Controlled Oscillators (VCO's) which cover the range from 100 MHz - 200 MHz, and a programmable frequency divider providing a division range from 2 to 2^{35}, resulting in a frequency range from 5 MHz to 200 MHz. The VCO control voltage is provided by a Phase-Locked Loop based Frequency Synthesizer.

The source of the 4 MHz reference frequency for the synthesizer may be selected from either an on-board Crystal or an external source connected to the 9100's rear panel CLOCK REF connector. The CLOCK REF input is AC coupled, and has a 51 Ω input impedance. The synthesizer will operate with input signal amplitudes from 500 mV to 5 V p-p and is programmable from 100 MHz to 200 MHz, in 62.5 kHz steps.

The lower frequency VCO works over a frequency range from less than 95 MHz to greater than 130 MHz. The middle range VCO operates from less than 120 MHz to greater than 165 MHz. The upper VCO runs from less than 155 MHz to greater than 205 MHz. In the 9100, low VCO is used from 100 MHz to 124.9375 MHz, the middle VCO from 125 MHz up to 159.9375 MHz, and the high VCO is used from 160 MHz to 200 MHz. Note that only one of the 3 VCO's should be enabled while a waveform is being generated.

The 9100-6 contains 2 separate frequency dividers. The first of these can provide division of the VCO frequency from ÷2 to ÷32 in power of 2 steps. The other divider provides division of the VCO frequency from $\div 2^{6}$ to $\div 2^{35}$, also in power of 2 steps.

Programming A Specific Frequency

The procedure for programming the timebase for a specific frequency is as follows: If the desired timebase frequency is below 100 MHz, multiply it by a power of 2 as large as necessary to obtain a number between 100 MHz and 200 MHz. The resulting number will be the frequency to which the VCO should be programmed, and the power of 2 multiplied by to obtain this number will be used to divide the VCO frequency down to the desired timebase frequency.

Suppose, for example, that a 100 Hz, single channel, sinewave containing 32 points is required. The desired timebase frequency is 3.2 kHz. Multiplying 3.2 kHz by 32768 (2^{15}) we obtain 104.8576 MHz. This is the frequency that the synthesizer will be programmed for.

Note: For dual channel outputs, the timebase is programmed for twice the point output rate.

Now we need to program the synthesizer to 104.8576 MHz. Because the step size of the synthesizer is 62.5 kHz, the closest we can get to this number is 104.875 MHz (62500 x 1678), which is what we will really program for. Since this frequency is less than 125 MHz, we select the low VCO range. Also, we will want to use

the higher-order frequency divider, to divide by 2^{15}. This will result in a VCO frequency of 104.875 MHz, a timebase frequency of 3.200531 kHz, and a sinewave output frequency of 100.0166 Hz, or an error in the desired output frequency of .0166%.

External Timebase Sources

One can also elect to bypass the internal timebase circuitry altogether and drive the AFG with an external source connected to the rear panel EXT CLOCK connector. This is a DC coupled input terminated in approximately 50 Ω, which drives a high-speed comparator through a x2 attenuator and a clamping circuit which limits the signal swing at the comparator input to about ±1.3 V. The comparator's threshold input is driven by an 8-bit DAC. The DAC output is programmable from -1.25 V to +1.25 V in steps of approximately 10 mV (2.5/255). Since the external signal delivered to the comparator is divided by 2, this results in an apparent external clock threshold range of ± 2.5 V, with resolution of about 20 mV. This means that if the user programs for a clock threshold level of 2 V, the actual comparator threshold will be 1 V. The maximum rate for an external clock signal is slightly in excess of 200 MHz. To utilize the external clocking feature, the comparator threshold DAC should be programmed to the approximate half-amplitude point of the intended driving signal. Additionally, be aware that all of the edge-triggered devices in the 9100-6's internal timing and logic circuitry respond to positive edges. If it is desired that the start and stop of the waveform output, and all waveform transitions, be referenced to the negative edge of the external clock signal, we can invert the applied clock signal by programming for negative clock slope.

Clock Output and Master/Slave Operation (Version 1.100 or later firmware)

Also available on the rear panel of the 9100 are 2 clock outputs. The signal at these CLOCK OUT connectors are NIM logic levels (see note below). The Clock 1 output is a free-running signal at the timebase frequency. The Clock 2 output is gated, running only when a waveform is running, and looks essentially like the invert of the clock signal delivered to the 9100-2 Analog Output card. This output is intended for use as the "master" clock signal when two or more 9100s are to be operated in master/slave mode.

NOTE: The NIM level is defined as -16 mA into a 50 Ω load when the output is true, and 0 mA into 50 Ω when false. This will result in a voltage of -800 mV in the true state, and 0 mV in the false state.

The following comments apply to master/slave operation:

1) **ON REV E AND OLDER BOARDS** - Because the master/slave operating mode was not implemented on the 9100-6 board until Rev F, the two clock outputs in 9100s containing -6 cards of Rev E and older will be identical to each other. As shipped,

these outputs will run at the programmed **internal** timebase rate, even if external clocking is selected. However, a jumper option is provided at the front of the card (just behind J608) which, if the installed shunt is moved to the forward position, will allow these outputs to be driven by whatever clock drives the rest of the card.

2) As mentioned above, **for dual channel operation, the timebase frequency is twice the point output rate.**

3) Any 9100 with the 9100-6 equal to rev. F or higher may act as a "master" in master/slave mode by connecting its Clock 2 output to another 9100 programmed as a slave. For absolute synchronization of master and slave outputs, it will be necessary to add a cable delay of about 20 nsec in the analog output(s) of the master unit, to compensate for the cable delay between master and slave and propagation delays in the slave unit.

4) The above only allows one 9100 to be slaved to one master. More can easily be slaved by inserting a NIM logic fanout between the master's Clock 2 output and the slaves' Ext Clock inputs. The LeCroy 429A Logic Fan-In and Fan-Out is ideally suited to this purpose if the user has a NIM instrumentation bin. Also, be aware that additional delay will need to be added at the master's analog output(s) to compensate for the delay of the fanout if absolute synchronization is required.

5) The clock outputs of units programmed as slaves will be completely uncorrelated to their waveform outputs, and therefore are probably not particularly useful.

Triggering

Waveform generation in the 9100 can be triggered from one of three sources; manually (by the front panel MANUAL TRIGGER pushbutton), by a command from the driving computer (referred to herein as bus triggering), or by an external source connected to the front panel TRIGGER/GATE INPUT connector. As far as the 9100-6 is concerned, manual and bus triggers are identical. Pushing the MANUAL TRIGGER button causes the 9100-3 board to generate an interrupt, which in turn causes the 9100's internal CPU to deliver a bus trigger command to the 9100-6.

Before the 9100 can recognize a trigger, the trigger circuitry must be armed. This can be done under user control (known as bus arming), or can be done automatically under hardware control (auto-arming).

The external TRIGGER/GATE INPUT impedance is approximately 50 Ω, and the input is DC coupled. A comparator is driven through a x2 attenuator and a clamping circuit limiting the signal swing at the comparator to around ±1.3 V. The comparator's threshold input is driven by an 8-bit DAC. The DAC'S output voltage is programmable from -1.25 V to +1.25 V in steps of about 10 mV.

Since the external signal delivered to the comparator is divided by 2, this results in an apparent external trigger threshold range of ± 2.5 V, with resolution of about 20 mV. This means that if the user programs for a trigger threshold level of 2 V, the actual comparator threshold will be 1 V. The DAC should be programmed for a comparator threshold voltage appropriate to the signal applied to the TRIGGER/GATE INPUT connector. The minimum trigger pulse width is 2 nsec. To utilize the external trigger, the input must first be enabled, i.e. the External trigger source must be turned on. Enabling the external trigger does not inhibit the recognition of a bus trigger.

Regardless of the trigger source, the triggering signal is delivered to the clock input of a positive-edge triggered D-type flip-flop. If the user wishes to trigger on the negative edge of his external trigger, he can invert the signal before delivery to the flip-flop by selecting a negative trigger slope. The actual start of waveform generation by the 9100 can be delayed from the recognition of a trigger by up to 1,000,000 cycles of the timebase clock. When the aforementioned flip-flop is clocked by a trigger, it passes a high to the data input of another D-flop, which is clocked at the timebase frequency. At the first positive clock edge after this input goes high, the start delay counter is allowed to count.

The 20-bit start delay counter is comprised of a fast 4-bit ECL counter (for the 4 lsb's) and 2 8-bit TTL counters. These counters are loaded with the 1s compliment of the number of timebase cycles of delay desired between the recognition of a trigger and the start of the waveform output. Note that this counter should not be loaded for zero delay (i.e. with all 1's). At least 1 cycle of delay is necessary for proper operation.

Actual waveform generation is commenced when the start delay counter reaches its maximum value. The first positive timebase clock edge after this event will enable the 9100-6's internal gated counters and start the delivery of clock signals to the analog and fast memory cards. Thus, the minimum delay from the recognition of a trigger to the first transition on the analog output is 4 timebase clock cycles, (1 to enable the start delay counter, 1 delay counter cycle, and 1 to open the gate for the gated clocks, and one more for the first clock output edge) plus about 50 nsec of internal propagation and cable delays.

The TRIGGER/GATE INPUT can also be configured to operate as a gate. In this mode of operation, the leading edge of the input pulse will trigger the unit as above, but waveform generation will stop at the first End-Of-Waveform condition after the trailing edge of the input signal. To use this input in this manner, one must first program the trigger threshold DAC appropriately for the signal to be applied, and then select trigger mode Gate.

Triggering Modes

The 9100 can output a programmed waveform in 1 of 5 different modes; continuous, recurrent, single, burst, or gated. Gated mode has already been discussed in the previous section. The remaining modes will be dealt with in this section.

In continuous mode, the programmed waveform is repeated indefinitely, until an abort command is received. In this mode the terminal count output of the waveform repetition counter, which is used to stop the clock, is inhibited. Thus, the clock never stops, and the waveform is repeated until halted by an abort. Note that waveforms of less than 72 points can only be generated in continuous mode.

In burst mode, the programmed waveform is repeated a programmed number of times, up to 65,535, each time a trigger is recognized. The 16-bit waveform repetition counter is comprised of 2 8-bit counters, loaded with 1s compliment of the desired number of waveform repetitions.

In single mode, the programmed waveform is cycled once per trigger. This is merely a variation of burst mode, with the repetition counter programmed for 1 (actually, the 16-bit 1s compliment of 1 which is FFFE hex or 65,534).

Recurrent mode is similar to continuous mode, except in that a programmable delay will occur between the end of each waveform cycle and the start of the next. In this mode the unit retriggers itself after the trigger reset period (10 timebase clock cycles) plus about 50 nsec. After the retrigger, the waveform output(s) returns to its (their) initial value(s). After the trigger delay period, the clock starts again and transitions can occur on the analog output(s). The minimum delay between the end of one recurrent waveform cycle and the beginning of the next is 16 timebase cycles. See Appendix B for more detailed trigger mode discussion.

Stopping The Waveform Output

A waveform stored in the 9100 can consist of up to 682 segments of a minimum length of 72 points. (Waveforms of less than 72 points can be generated, but these short waveforms can only consist of a single segment, minimum length 8 points, and can only be generated in continuous mode. Linking of short segments is not possible.) The end of a given waveform is obviously, the last point of the last segment. One of the major functions of the -6 board is to know when a given waveform has reached its end, and to stop providing clock signals to the other cards at that time. To facilitate this function, the Fast Memory card (9100-1) sends 3 signals to the -6. One of these signals provides clock pulses to the -6's Waveform Repetition counter, one occurs when the -1 has begun to output the last segment of a waveform, and one happens when the -1 begins to output the

last 8 bytes (points) of a segment. These signals will be referred to herein as WaveRepClk, EOW (End-Of-Waveform) and EOS (End-Of-Segment). In the following section, we will examine how the 9100-6 uses these signals and its internal logic to determine where to stop a waveform.

The above mentioned EOW signal is logically combined with 2 internally generated timing signals in the 9100-6, and the output of this network drives the data input of a D-type Flip-Flop, known as the Stop Flop. This data will be true when:

1) The 9100-6 receives an EOW from the 9100-1...AND... the Waveform Repetition Counter has reached its overflow value (i.e. the programmed number of repetitions for a Burst (or Single) Mode output has been reached).

OR

2) The 9100-6 receives an EOW from the 9100-1...AND... the Gate input goes to its false state (in Gate Mode).

So, when the data at the Stop Flop is true, the 9100-6 knows that it is clocking out the last segment of the waveform currently in memory. Now, all it needs to know is when the last point of this segment occurs so it can stop sending clock signals.

The 9100-6 contains an 8-bit ring counter, whose output is a pulse 1 timebase clock cycle wide, which keeps track of potential segment boundaries. Since each segment must be some multiple of 8 points wide, the last point of any given segment must coincide with the output of this counter. The output of this counter is AND gated with the EOS signal from the 9100-1, and the output of this gate drives the clock enable input of the Stop Flop. When this input is enabled, the next positive timebase clock edge will transfer the EOW data to the Stop Flop's output, which is wire-OR'd with the clock output stage's driving signal. This is how the stop condition is detected by the 9100-6, and the waveform output brought to an end at the proper point.

Events Subsequent to Stop Condition

What occurs after the waveform has stopped is dependent on the states of several of the 9100-6's control bits. In particular, if the auto-arm bit is not set, nothing will happen at all until an Arm command is issued.

If the auto arm bit is set, or after an Arm command has been received, the reset counter is enabled. A trigger reset cycle, which is 10 timebase clock cycles long is then commenced. During this time, the triggering chain is re-initialized, and the start delay, marker delay, and waveform repetition counters are re-loaded with the whatever numbers happen to reside in their respective holding registers. The stop flop is returned

to its initial state at the end of this period. After the completion of this reset cycle, the trigger is re-armed and the 9100 is again ready for a new trigger.

If the re-trigger bit is set, the 9100-6 will generate a new trigger itself, occurring 2 timebase clock cycles after the end of the reset period (see the discussion of recurrent mode in the section on triggering modes above). The 9100-6 responds to this internally generated re-trigger exactly as it would to an externally generated one.

User Timing Outputs

The 9100-6 provides 4 timing outputs that a user can utilize to synchronize any devices following the AFG in his measurement system. These are the SYNC, START, and MARKER outputs, available on the 9100's front panel, and the 2 rear panel CLOCK OUT signals. The CLOCK outputs were discussed in the Timebase section above. The other three outputs will be discussed below.

The SYNC output is a pulse, approximately 75 nsec wide, at TTL logic levels into a high impedance, or about 1.5 V into 50 Ω, which occurs 2 timebase clock cycles, plus about 30 nsec of internal propagation delay, after the recognition of a trigger. This output is useful for synchronizing external instruments to the 9100's trigger circuitry, since there is a full timebase cycle of uncertainty between the receipt of an external trigger and its recognition. This output should be used instead of the external trigger generator, for example, as the oscilloscope trigger for looking at an AFG output in externally triggered single or burst modes. Note that only a single pulse will occur on this output in continuous mode, after the bus trigger that starts operation.

The waveform START output is a pulse similar to the SYNC output in characteristics, occurring about 30 nsec after the 9100-6's gated clocks are enabled, i.e. after the programmed trigger delay has expired and the waveform output is about to commence. This is also the only one of the front panel outputs which is active when the 9100 is in Continuous Mode. The width of the Start pulse is only about 25 nsec in Continuous mode, so that one pulse can occur on this output for every repetition of an 8 point waveform at a 200 MHz timebase rate. In all other trigger modes, the Start pulse will be about 75 nsec wide.

The MARKER output is also similar to the SYNC and START outputs in characteristics, and occurs a programmed number of clock cycles after the receipt of a trigger, plus around 30 nsec. A 20-bit counter, similar to the start delay counter (see the section on Triggering above) supplies the delay. Like the SYNC pulse, this output will occur only once when a Continuous Mode output is being generated.

Adjustments on the 9100-6

There are several adjustments on the 9100-6 board, but most of these are factory preset and not to be adjusted except at the factory. The only adjustment available to the user is the adjustment for the reference frequency that the timebase is locked to. This adjustment calls for a fair amount of disassembly and should not be attempted casually. (See CHAPTER 3, SECTION V).

5.2 GROUP II - PROCESSING AND CONTROL (The 9100-13 and 9100-3 combination)

These two boards together accomplish the following functions;

1) Control and sequencing of all Model 9100 functions except actual waveform generation

2) Control, storage and retrieval of all commands, files and user inputs and outputs, except the actual analog output and the timebase signals delineated above.

3) The decoding, encoding and movement of these commands, files and inputs and outputs via the Multibus interface

4) The control of the data flow to and from the waveform generation group.

5.2.1 The 9100-13 Single Board Computer, System CPU

Note: The 9100-13 may only be installed in the bottom slot of the mainframe.

Functional Desciption

Figure 5-8, details the major functional blocks of the 9100-13, as follows:

1) The 80186 CPU and DMA controller which is the Model 9100 System central processing unit.

2) The 8087 Numeric Coprocessor which is a system option.

3) The local memory sites which contain on_board memory and the PROMS which hold the system firmware.

4) The Multibus interface which has been described above.

5) The ilbx and isbx bus interfaces, which are not used in the Model 9100 system implementation.

6) The RS232 interfaces which are shown above in Figure 5-1.

7) The 8255 parallel interface which is utilized for the 9100-10 Rear Panel Switches (See 9100-5 discussion below).

8) The other internal functions such as local data bus, interrupts and control logic which are not detailed in the manual.

User Serviceable Parts 9100-13

There are no user seviceable parts or adjustments on the 9100-13. PROM changes for firmware updates or options can be changed by user personnel. The procedure for PROM change is detailed in paragraph 4.6 above.

5.2.2 The 9100-3 Static RAM

Functional Description

The 9100-3 is a Multibus compatible board which provides the three system functions of:

1) System and file memory as 512k of 32k x 8 static memory chips including the battery backup circuitry for this memory.

2) Interface function for the GPIB hardware

3) Interface function for the 9100-9 Front Panel Subassembly

These functions are shown in detail in the 9100-3 schematic in Appendix B.

System Memory Function

The memory is 512K bytes of static RAM made up of two banks of 32KX8 (HM62256) memory I.C.'s operating in a ping pong fashion. One bank makes up the high order (odd) bytes U1-U8. The other provides for low order (even) bytes U9-U16. The memory is either byte (8 bits) or word (16 bits) addressable selected by BHEN and A0 (see Schematic for 9100-3) and Figure 5-9 below.

DATA XFER	BHEN	A0
Even Byte	1	1
Odd Byte	1	0
Word	0	1

Figure 5.9

The memory is completely battery backup using two 1.2 V Nicads in series providing a sufficient backup voltage of 2.4 V (see Battery Backup Section).

CR6 and Q1 provide a disable for the decoder (U18) when supply voltage drops below 4 V. The purpose is to inhibit the micro-processor from writing garbage data into memory under low voltage conditions.

Battery Backup Function

The 9100-3 provides complete battery backup for 512K byte static RAM using two 1.2 V Nicad batteries in series. The battery backup scheme incorporates a fast charge circuit for when batteries are below normal operating voltage as well as a trickle charge current to keep batteries at full charge.

The fast charge circuit is made up of U51 (REF02) and U52 (TL084) which establish the voltage charging reference for both the positive and negative batteries (battery considered negative with respect to common Pin 3, J1). The fast charge current is developed by U55, CR4 and Q2 for the positive side and U55, CR5, and Q3 for the negative side. When power is on approximately 154 mA of charge current is produced to bring the batteries up to normal operating voltages. When batteries are fully charged Q2 and Q3 FETs open cutting off the fast charge current. Once the FETs open R22 and R23 produce a small amount of trickle current (approximately 9 mA) sufficient to keep Nicads fully charged.

There is also a battery low signal (BATLO) to a front panel LED produced when the reference voltage at Pin #3 of U52 drops below 1.17 V triggering U53 and U54 (see Warning). In the case where non-nickle Cadium batteries are used jumpers P3, J3 and P4, J4 must be in the ground position to disengage the fast charging circuit. Q6, Q7, Q8 and Q9 also produce the BATLO signal if batteries are installed backwards or if only one or no batteries are installed.

*******WARNING:********

Do not turn unit off if battery low LED is on. This indicates insufficient battery backup voltage which will cause any information in memory to be lost.

GPIB Interface Function

The General Purpose Interface Bus (GPIB) is designed to allow 15 instruments within a localized area to communicate over a common bus. Each device has its own address read from external switches (see Rear Panel 9100-5 Section) at power on. Information is transmitted in byte serial format and may consist of either device-dependent data or interface commands.

Data may be sent by any one device (talker) and received by a number of other devices (listeners). One of the devices on the bus, designated the controller in charge (controller), may send interface control messages. Devices can be assigned to the bus

as listeners or talkers by sending their individual talk or listen addresses.

U26 (TMS9914A) provides an interface between the microprocessor and the General Purpose Interface Bus (GPIB) specified in the IEEE488 Standard. U21 (75160) is the transceiver for the eight data lines and U20 (75162) is for control signals and handshaking.

Front Panel Interface Function

The interface between the 9100-9 Front Panel switches and indicators is shown on the schematic.

9100-3 Battery Charger/Detector Test Procedure

Voltage Threshold Adjustments

a) battery charger reference:

turn pot R34 (1K) such that the voltage on pin U52-5 (TL084) is 1.3 V.

b) battery low detector reference:

turn pot R32 (1K) such that the voltage on pin U52-3 (TL084) is 1.17 V.

Charging Currents Measurements

a) fast charge:

NOTE: batteries must be removed for this test!

- remove jumper J3 from P3
- install the positive current meter probe on left pin of P3 (the one that is next to Q3)
- ground the negative current meter probe
- the charging current should be 154 mA with a 10 mA tolerance
- remove jumper J4 from P4
- install the positive current meter probe on left pin of P4 (the one that is next to K2)
- ground the negative current meter probe
- the charging current should be 154 mA with a 10 mA tolerance.

b) trickle charge:

NOTE: batteries must be installed for this test!

- remove jumper J3 from P3
- install the current meter probes where jumper was removed (in charge position)

- the charging current should be 9 mA with a 1 mA tolerance
- remove jumper J4 from P4
- install the current meter probes where jumper was removed (in charge position)
- the charging current should be 9 mA with a 1 mA tolerance

Battery Low Indicator Status

- check the front panel BATTERY LOW LED with the following jumper and battery configurations:

Battery Low	J3	J4	Left Battery	Right Battery
-	charge	charge	in	in
off	charge	charge	in	out
on	charge	charge	out	in
on	charge	charge	out	out
on	N.C.	N.C.	in	in
off	N.C.	N.C.	in	out
on	N.C.	N.C.	out	in
on	N.C.	N.C.	out	out
on				

Static RAM Voltage

NOTE: batteries must be installed for this test!

- shut off the power to the AFG

- with a voltmeter measure the voltage on pin U1-28; it should be 2.4 V with a maximum limit of 2.8 V.

5.3 GROUP III - STATUS INDICATION, SWITCHES AND EXTERNAL CONNECTION (The 9100-9 Front Panel and 9100-10 Rear Panel)

5.3.1 9100-9 Front Panel

FRONT PANEL INDICATORS

The 9100-7 front panel board indicates the various functions of the 9100 AFG. It is controlled by the 9100-3 static RAM/GPIB interface board. The 9100-3 provides the front panel chip

selects and necessary Multibus interface functions to allow the 9100-13 computer board to control the actual status of the light emitting diodes(LEDs) and to select between the various input connections. As previously discussed most connections are made directly to the GROUP I - WAVEFORM GENRATION BOARDS.

The following is a list of the front panel LED's and their descriptions.

LED	**DESCRIPTION**
Self Test	When this LED is on (at power up) it indicates that the 9100 AFG is going through self calibration of on board DACs (9100-2 board). If it is on in response to 'SELFTEST' command, it indicates a complete selftest in progress.
Test Fault	If this LED is on it indicates a problem with the micro processor meaning that the MPU did not update within the prescribed 10-15 seconds set by monostable U1 (74LS123). This LED flashes for 10 seconds after CALIBRATE or SELFTEST detect errors.
Local	When on this LED indicates that all 9100/CP hand held controller functions are available.
Battery Low	When on this LED indicates an insufficient amount of battery backup voltage (see 9100-3 Battery Backup Section). It could also indicate that batteries are installed backwards or that only one battery or no batteries are installed. (If battery low LED is on see warning in 9100-3 Battery Backup Section).
GPIB SRQ	When on the Service Request (SRQ) LED indicates that the 9100 AFG is requesting the controllers attention. The controller responds by asserting attention (ATN) and executes a serial poll to determine which instrument is requesting service, and why. When polled the 9100 AFG unasserts the SRQ line.
GPIB Listen	When on this LED indicates that the 9100 AFG has been addressed as a listener and may receive data over GPIB.
GPIB Talk	When on this LED indicates that the 9100 AFG has been addressed as a talker and may send data over GPIB.

CHAN "1"Invert	When on this LED indicates that the Channel "1" output inversion is enabled.
CHAN "2"Invert	When on this LED indicates that the Channel "2" output inversion is enabled.
CHAN "1"	When on this LED indicates that the Channel "1" output is enabled. When flashing an overload has occurred on the channel output.
CHAN "2"	When on this LED indicates that the Channel "2" output is enabled. When flashing an overload has occurred on the channel output.
SUM "1+2"	When on this LED indicates that the internal channel sum is enabled. The Channel 1 output is the sum of the Channel "1" and Channel "2" signals. When flashing an overload has occurred on the external sum input.
Armed	When on this LED indicates that the 9100 AFG is ready to accept a trigger (manual or external if selected).
Waveform Active	When on this LED indicates that the actual desired waveform is either waiting for trigger or being generated at the selected output. This LED is on between "GO" and "ABORT".
Power	Indicates that power is on.

FRONT PANEL SWITCHES

The **MANUAL** trigger switch and the **SELFTEST** switch also interface via the 9100-3 board. Operation of these switches is discussed in the Model 9100 Operator's Manual.

FRONT PANEL CONNECTIONS

The Front Panel connections to the 9100-2 and 9100-6 boards are discussed above in the sections describing these boards.

5.3.2 9100-10 Rear Panel Assembly

The Rear Panel provides the following mechanical and electrical functions for the Model 9100 AFG;

1) Mechanical - Fan Placement and battery case location and primary power connection. Additional, both the RS232, GPIB, and timing (clock) in/out connections are provided, as previously discussed.

2) Electrical - Voltage Selection, RS-232 and GPIB Switches.

Voltage Selection

See Voltage Selection Warning in CHAPTER 2, above.

9100-5 RS-232 and GPIB Switches

The 9100-5 is the simplest subassembly in the Arbitrary Function Generator. It consists of two 8 position DIP Switches. One sets the RS-232 parameters and the other is for selecting General Purpose Interface Bus (GPIB) parameters. The functions and setting of these switches is detailed in the Model 9100 Operator's Manual.

5.4 GROUP IV - INTERNAL CONNECTION AND POWER DISTRIBUTION (9100-4 Backplane and 9100-8(Card Cage and Power Supply)

As discussed above both these function are provided by the Multibus backplane and there are no user serviceable adjustments associated with this subassembly. Power Supply details are discussed in CHAPTER 6 - TROUBLESHOOTING.

CHAPTER 6

TROUBLESHOOTING GUIDE FOR THE 9100

6.0 Introduction

In order to help simplify servicing and minimize downtime the following list of possible symptoms, likely causes, and troubleshooting steps have been prepared.

Note: Most procedures in this section will allow a technician to troubleshoot down to the board level. Defective circuit boards will be repaired or exchanged by your regional LeCroy Service Office.

A complete list of recommended service equipment and spare parts is in Section 1.2 of this manual.

6.1 Basic Troubleshooting - Connections and Power Supplies

It will not be necessary to rearrange or remove any circuit boards at this time. Connect the 9100/CP to its front-panel jack. Connect the computer if you have one. Now apply power to the 9100.

The first step in troubleshooting is to check for obvious items like blown fuses, voltage selector switch in correct position and loose line cord. The power supply is the next item to check before proceeding to more detailed troubleshooting. Noisy or low power supply lines can cause a variety of problems, both digital and analog.

Remove the top cover. The power supply lines come into the motherboard at the lower right side, and test points are labelled on the upper right corner of the motherboard. The test points are +15, -15, +12, -12, +5 and -5.2 volts. They can be easily measured with a DVM.

Older 9100s may not have the labelled test points. On these units the supply lines come into the motherboard at the upper right, and may be measured with a DVM. Below is a list of wires and their supply voltages.

Black	Voltage returns
Green	Ground
Violet	-15 V
Blue	-5.2 V
Red	+15 V
Orange	+5 V

If no voltages are present, the line fuse inside the power supply may be open. It is a 5 x 20 mm Type F 5 amp fast acting

fuse. Disconnect the 9100 from AC supply before attempting to access this fuse.

Power supply noise is measured with the bandwidth limit of the oscilloscope set to 20 MHz, and a 10:1 probe. The probe ground must be connected as close as possible to the voltage being measured, bayonet tip probe is preferred (don't just connect it to the frame) and the oscilloscope input should be set for AC coupling. The ripple should be less than 1% of the nominal voltage of the line being measured. Ripple may be present at 120 Hz and/or at 100 KHz, the switching frequency of the power supply. If the power supply looks OK, proceed to look up the problem on the table which follows.

6.2 Typical Problems and Their Symptoms

SYMPTOM: No Response to Control via 9100/CP

If the "Local" LED is not lit the unit is likely in the remote mode. Depress the local key on the CP, if the "Local" LED doesn't turn on recycle the power to see if the "Local" LED comes on. If the "Local" LED is on, make sure you have +5 V coming into the 9100/CP. At this point drop the front panel to service position. The power for the CP is easily measured at the block connector that connects to the power switch. The +5 V is carried by the orange wire at the extreme lower left of the connector. If the voltage is not present there, but you are getting +5 V out of the power supply, the fuse directly below the block connector is probably blown. Remove the fuse and measure it with an ohmmeter. Replace with a 1A 250 V 3AG type fuse.

If the power supply voltages are present and the 9100/CP beeps when a key is depressed, check the connection from the 9100/CP to the 9100-13. If all connections are good, then the 9100-13 is defective and should be exchanged for another one.

If the voltages are present and the 9100/CP does NOT beep when a key is depressed, the 9100/CP is defective and should be exchanged for another one.

SYMPTOM: No Response to Control via GPIB

The most obvious thing to check first here is that the GPIB address that the program is trying to access agrees with the GPIB address for which the 9100 is set. The GPIB address will appear on the 9100/CP along with the version number of the PROMs in the unit upon completion of the power up self-check. If the addresses agree, then further checking is necessary. First, make sure the actual switch settings on the rear panel correspond to the address the 9100/CP displays after the power up self-check. If they do not match up, measure the continuity of the GPIB

address switches with an ohmmeter. Note that the 9100 reads the rear panel switches at power up only; it is therefore necessary to turn the unit off and on after changing the GPIB address.

If the switches are okay make sure that cable number 19 is connected properly to the 9100-3 and cable number 21 is connected properly to the 9100-13. If there is no problem with the cables and switches, but the 9100 is still operating as if it is set at a different address than is indicated by the switch settings, the problem lies with the 9100-13.

If the address is displayed by the 9100/CP after power up agrees with the address that is set on the rear-panel switches and unit does not respond properly to GPIB commands, the problem most likely lies with the 9100-3, which contains the GPIB interface circuitry.

When using LeCroy EASYWAVE make sure the GPIB address matches AFG address. GPIB problem may also be with the host computer.

NOTE: Due to incompatability of the P2 connector the 9100-13 (CPU) board can not be placed in other than bottom slot.

SYMPTOM: No Analog Output - CHANNEL 1 or CHANNEL 2

Remove top cover and unscrew front panel for debugging access. Reset or repower the AFG. Activate a dual square wave from standard functions. Connect CHAN 1 and CHAN 2 outputs to a scope and trigger the scope on the START output. There should be a 1 V p-p square wave into 50Ω termination with offset of 0 V at 1 MHz on both outputs. Determine if both or one output is missing.

The top board is the 9100-2 (analog board). This board generates an analog signal for 1 or 2 channels from a digital code.

NOTE: All front input signals (coax and flat cable) to 9100-2 board are ECL levels. When service cable kit is available, place 9100-2 on a extender for easier access to probing points.

At first examine all interboard cable connections for loose cables.

If one output is missing check for square wave on 9100-1 on U35 pin 2 for channel 1 and U36 pin 2 for channel 2 (U35 and U36 are HFA100), if the square wave is present the problem definitely exists in 9100-2. If the signal is not there the digital data must be checked, the data comes from 9100-1 (board below) via two 34 conductor cables. The data bus can be accessed on top side of 9100-2 board on U19 U20 U23 and U26 pins 3, 2, 1, 24, 19, 18, 17, and 16 of each chip mentioned above (these IC's have heatsinks on them). Probe those points for data of 1 MHz at

ECL levels. If data is present it further verifies that the problem exists on the 9100-2, if data isn't present check it on the 9100-1 by probing solder side of headers; if it is not present there the problem exists on the 9100-1.

When missing one channel and signal exists on HFA100, you may be able to isolate the problem to an HFA100 or an amplifier hybrid. With the 9100 turned off, swap the HFA100s to see if the problem moves with the HFA100. You may also swap U37 and U38 to see if the problem moves with these hybrids.

If both channels are missing follow the procedure described above. In addition check CLOCK and LOAD signal (Figure 6.1) coming to 9100-2 board, if these signals are not toggling the problem most likely exists in 9100-6. Also check for clock on 9100-1 (SMB in center of the board) if signal is not present the problem lies in the 9100-6. Check for blown fuses on all three boards 9100-1, 9100-2, 9100-6 boards located close to P1 in each case.

NOTE: If Channel and Waveform Active LEDs Fail to Light

If the appropriate LEDs fail to light when troubleshooting for missing output(s), then you may have more than one problem. The front-panel LEDs should all light on power up self test, with the exception of the "Battery Low" LED. If these fail to light on power up test, either the 9100-13 CPU board is not correctly executing its program (which could indicate one of a number of problems) or you have a problem with the 9100-3.

SYMPTOM: Analog Outputs Seem Distorted

High Total Harmonic Distortion (THD)

High THD very likely points to a problem within 9100-2. Damaged or incorrectly biased output protection circuitry can contribute to higher THD. To check output protection circuit activate a dual sine wave from standard functions using 9100/CP or using EASYWAVE. Connect variable output power supply to CHAN 1 output and slowly increase the voltage, the output should trip at approximately 14 V and it will be indicated by flashing CHAN 1 LED. IF the output trips much before the 14 V threshhold then the output protection circuit is probably contributing to higher THD. Check protection against both positive and negative externally applied voltages. Follow the same procedure for CHAN 2. If the problem mentioned above exists then the 9100-2 should be replaced.

Another source of distortion on the waveform output is offset vs. amplitude being out of range. Refer to USER MANUAL for those limits. If waveform should be within limits it is likely that

the internal calibration has failed. See "DC or AC Calibration", discussed later in this chapter.

One more problem that may be contributing to high THD is one or more missing bits. Run a dual sine wave from standard functions and examine it on a scope for smoothness, there only should be digital steps visible. If a step seems more out of line than usual then check for dropped bits. Refer to section entitled SYMPTOM: No Analog Output - CHANNEL 1 or CHANNEL 2 to follow how to check for missing bits procedure.

SYMPTOM: Analog Outputs Noisy

If the noise on the analog outputs is exceeding the specs and the power supply is ok then most likely the 9100-2 board is bad and should be exchanged. Make sure that what you are seeing is noise and not a bad bit.

SYMPTOM: DC or AC Calibration of Output Incorrect

NOTE: To see calibration results a CALERR.SEQ file can be read via the RS232 port. To do this power up in RS232 by setting GPIB dip switch position 3 switch down. Hookup a RS232 terminal and at prompt AFG> type recall,calerr.seq;. If calibration was successful the return message will say so if not calibration errors will be displayed. (CALERR.SEQ may also be read out over GPIB. but an introduction to GPIB is beyond the scope of this manual.) Note that EASYWAVE® can display CALERR.SEQ in file transfer.

If the DC calibration of the analog output is out of spec, the first thing to check is the termination resistor is in tolerance (this will not be detected by calibration). Also check cable 6 and 7 for loose connections. Another possible cause is excessive resistance across the contacts of the output relay. This can be confirmed by measuring the voltage drop across the relay.

To generate a signal to make DC measurements, power up and using the 9100/CP or EASYWAVE activate dual DC wave from standard functions. Connect CHAN 1 output to a DVM and terminate into 50 Ω. Go to CHAN 1 offset menu and increase or decrease the offset with default values.

SYMPTOM: CLOCK IN or CLOCK OUT Not Functioning Correctly

If the EXT CLOCK input does not appear to be functioning properly make sure that the signal connected to it meets the specifications. The signal should be a square wave of 5 nsec period for our tests. This will correspond to a clock frequency of 200 MHz. Please bear in mind that the rear panel CLOCK OUTPUTS are not slaved to the EXT CLOCK input, even if the external clock source is selected. Make sure you have the CLOCK LEVEL set for 50% of the clock input signal amplitude. Also be sure that the period is 5 nsec or greater (200 MHz or less). At clock frequencies greater than 200 MHz the output of the 9100

will break up and become distorted. After you have checked all these criteria load a waveform and run it. Switch between internal and external clocks. You should see no difference in the output of the 9100 as displayed on an oscilloscope. The only acceptable difference will be a difference in the frequency of the AFG output signal which would be due to the internal and external clocks being set at different frequencies. If there are other differences, the 9100-6 must be replaced.

If there is no waveform output with either internal or external clock selected, make sure you have a CLOCK OUTPUT on both connectors (one and two) on the rear panel. These signals should swing from 0 V to -800 mV when driving a 50 Ω load. If these signals are missing or at the wrong levels, the 9100-6 is defective and must be replaced.

SYMPTOM: Triggering Not Functioning as Expected

The first thing one should check at this time is the possibility of set up error. Make sure the 9100 is set up correctly for the task you want it to perform. If you are not sure that the unit is set up correctly, refer to the 9100 Users Manual.

If all is set up correctly, and the trigger and timebase outputs are still not behaving as expected, there may be a defect in the 9100-6. If the front panel is not dropped down into the service position, put it into the service position. Examine the SMB connectors on the front of the 9100-6, and make sure they are fully inserted into their sockets. If all is well with the connections of the 9100-6, and the 9100-6 is fully inserted into the backplane, then the 9100-6 must be exchanged.

SYMPTOM: Test Fault LED Lighting

The Test Fault LED is under the control of the 9100-13 (the CPU). If this LED lights the 9100 will probably not perform any functions because this LED indicates a fault in the execution of the 9100s internal software. If the LED lights, and nothing else appears to be wrong, there is a slight possibility there is a fault in the 9100-7, which is the front panel display unit.

If the Test Fault LED is illuminated, and the 9100 does not respond to any commands, the CPU is not executing the software properly. The first step is to make sure all boards are inserted into their sockets in the 9100 backplane. If this does not cure the problem, remove the 9100-13 and examine it. Make sure that the PROM's are correctly inserted in their sockets and that the jumpers are in their proper places. If nothing appears to be incorrect on the CPU card, replace it with another. If the problem persists, get in touch with your regional LeCroy Service Office for assistance.

SYMPTOM: Battery Backup Not Working Properly

The battery backup circuit will directly affect the integrity of data stored on the 9100s internal RAM disk. If the data is being corrupted, and the Battery Low LED is not illuminating the defect is on the 9100-3. If the Battery Low LED is on, the first thing to check is that the batteries are putting out the correct voltage. You should measure between 2.4 V and 2.6 V on the pair of batteries in series with the power off. If this voltage is low there is either a defective battery or a defective battery charging circuitry. To determine which is defective proceed as follows:

Place a 50 Ω load across the inputs of a DVM. With the power to the AFG turned on, disconnect the unit's batteries. Now, using the DVM with the 50 Ω load connected across the inputs, measure the voltage being delivered by the charging circuit. This is most easily measured at the red and black wires coming from the front-panel display board. The measured voltage should be at 2.4 V to 2.6 V. If no voltage or a low voltage is present, the 9100-3 is defective and must be replaced. If the voltage is correct and the battery backup circuit is not working correctly, the most likely cause is the batteries.

CHAPTER 7
TEST AND RECALIBRATION AFTER REPAIR

7.0 Introduction

Due to the advanced design of the 9100 Arbitrary Function Generator calibration requirements have been reduced to absolutely minimal levels. For most users this means that periodic verification of calibration is all that would be required.

7.1 Internal Adjustments

Internally there is one available adjustment which will affect calibration. This is limited to a narrow range adjustment of the timebase reference.

The DC accuracy of the unit is guaranteed by an internal high precision reference and an ADC. In general, if the unit fails a calibration verification, it is likely that the unit needs to be serviced, not recalibrated. CHAPTER 3 provides procedures for verifying analog specifications. If the DC calibration of the analog output is visibly incorrect the 9100-2 is probably defective.

It is also possible that a timebase error could be causing the output to be distorted. This can be caused by instability of the timebase, causing the timing of the output to be skewed, or the timebase could be running at the wrong frequency, causing timing errors in the output. Fortunately, this is simple to check using a width of 10 nsec and a period of 40 nsec. You should see evenly spaced pulses every 100 nsec. Using the DELTA command, step through the pulse period making sure the period stays correct as displayed on the delta function to step through the period of the pulse, all the while checking the oscilloscope display for correctness of timing. Any defects in timing will be caused by the 9100-6.

7.2 Testing After Repair

After repair the recommended Test sequence would be to perform the tests in Chapter 2 (2.2, 2.3 or 2.4 whichever is most convenient), all of Chapter 3 and the Quick Test Procedure which follows.

7.3 9100 Series Quick Test Procedure

The procedure listed below should be performed on any unit that has been opened for service. Its purpose is essentially to verify that all system interconnects have been properly made and that all inputs and outputs are "alive".

I) Power up AFG without CP connected. Connect Sync output of AFG to external trigger input of scope, terminated in 50 Ω. Select external triggering on scope & set trigger level to ≈ .75 V. Connect AFG's channel 1 & 2 outputs to scope's channel 1 and 2 inputs, terminated in 50 Ω. Connect the AFG's trigger input to an external signal generator set for a 1 V positive-going pulse output, at a frequency of about 50 kHz.

II) In Easywave, download the files "testup.seq" and "testup.set" to the AFG, and run the sequence file (a listing of what these files should contain can be found at the end of this procedure).

III) When the file has finished running, the AFG should be generating a burst of 4 ramps on each channel in response to each trigger. Each ramp should be 2.56 μs in duration. The waveform on channel 1 will be at -.5 V quiescently and ramp up to +.5 V. The waveform on channel 2 will be at +.5 V quiescently & ramp down to - 5 V.

A) Disconnect the AFG's channel 2 output from the scope and connect the Start output. This pulse should be ≥ 1.5 V in amplitude, 50 - 100 nsec wide, and should occur at the start of the first ramp in the burst.

B) Disconnect the Start output from the scope and connect the Marker Output. This pulse should also be ≥ 1.5 V in amplitude and 50 - 100 nsec wide, and it should occur at the start of the third ramp in the burst.

C) Connect the Clock 1 output (rear panel) to a frequency counter. Disconnect the Marker from the scope & connect the Clock 2 output. Counter should read 200 MHz. Clock display on scope will depend on the Rev. level of the -6 card the unit under test contains. If the -6 is Rev. E or older, the clock will be running continuously at 200 MHz. If the -6 is Rev. F or newer, the clock will be active at 200 MHz only during the time that the ramps are present at the outputs, and will remain in the low state while the outputs await the next trigger.

IV) Exit Easywave and plug in the CP. Check that proper boot message is displayed, & that GPIB address is 1. Flashing Run/Stop cursor on lower right should be R. Set an external DC supply to 1 V and connect it to the Sum input. Disconnect the Clock from the scope and connect the channel 2 output.

A) Use CP to turn Xsum on. Check that channel 1 output offset shifts appropriately, & that channel 2 offset does not change. Turn Invert off in channel 2, and Xsum off and Sum on in channel 1. Channel 1 Offset should return to 0, and amplitude should double. Channel 2 output should be clamped at ground. Check front panel LEDs for proper channel status information (Chan 1 & Sum 1+2 LEDs on, Chan 2 LED off). Turn Sum off & both outputs should resemble the original channel 1 output.

B) Use CP to change Clock Ref to external. Rep rate of bursts should remain the same, but duration of burst should increase. Frequency counter should indicate a frequency between 130 and 160 MHz. Connect a 4 MHz sinewave to the rear panel Clock Ref input. Frequency should return to 200 MHz & burst output should appear as before. Change Ref source back to internal and disconnect Ref input. Connect this signal to the Ext Clock input.

C) Use CP to change Clock Rate to 4 MHz. Frequency counter should display 8 MHz, since a dual waveform is being generated. Decrease trigger rate to about 1 kHz. Burst duration should now be 256 μs (64 μsec/ramp). Change Clock Level to 0 V and switch Clock Src to external. Ramp and burst duration should double (128 μsec/ramp, 512 μsec/burst), but burst frequency should remain the same (≈ 1 kHz).

V) Use CP to change the waveform to a Standard Function Dual Square wave, running at 50 MHz in Continuous Mode. Trigger scope on AFG's Start output. If no output appears, check connections of the analog clock & analog load cables between the -6 and the -2.

VI) Turn off AFG. Set rear panel DIP switches for RS232 control and 1200 Baud. Set GPIB address to 14. Run Xtalk with Baud Rate set to 1200. Turn on AFG. Check boot screen on CP and make sure GPIB address now reads 14. Type:

recall calerr.seq;

The returned information should start with #I & be otherwise totally legible. Type:

comm_help,on;

Push the Self-Test button on the AFG's front panel. Test results will be reported on the terminal and all tests should pass.

VII) Power down AFG, return the DIP switches to their normal settings, and visually check to make certain that all the boards are locked securely into their slots. Information on spec verification can be found in Chapter 3 of this manual. Proper operation of the various triggering modes can be verified using the information in Chapter X.

Listing of the file testup.set:

```
#IC1A 1.000000E+000;C1O 0.000000E+000;C1F OFF;C1P ON;C1I OFF;C1Z
1.275000E+002;
SUM OFF;XSUM OFF;
C2A 1.000000E+000;C2O 0.000000E+000;C2F OFF;C2P ON;C2I ON;C2Z
1.275000E+002;
CSOU INT;CRAT 1.000000E+008;CLEV 2.000000E+000;CSLO POS;CREF
INT;
TMOD BURST,2;TAS AUTO;TSOU BUS,ON;TSOU EXT,ON;TSOU MAN,ON;
TLEV 5.000000E-001;TSLO POS;DMOD PTS;TDEL 4.0;MDEL 515.5;
SMOD    SING;SIFR    1.000000E+006;SC1P    0.000000E+000;SC2P
0.000000E+000;
SQMD    SING;SQFR    1.000000E+006;SQUP    0.000000E+000;SQRP
0.000000E+000;
TRIM    SING;TRFR    2.000000E+005;TRIP    0.000000E+000;TRRP
0.000000E+000;
RMOD    SING;RPER    4.000000E-003;RMPP    0.000000E+000;RPRP
0.000000E+000;
PPER    2.000000E-005;PWID    1.000000E-006;POPT    WID;PDEL
1.000000E-007;
DCMD SING;
END;
```

Listing of the file testup.seq:

```
#IArb;
Load a.wad,2;
Set Testup.set;
Go;
END;
```

CHAPTER 8

INFORMATION ON GPIB (General Purpose Interface Bus)

8.0 Introduction

This section is a simple description of the GPIB interface as an aid to understanding the interface in the 9100 AFG. It is not intended as a complete specification of the system.

The GPIB system is designed for the operation of a number of interacting devices, which may transmit or receive information as required. The system includes data lines over which the actual data are sent, bus management lines for control, and handshake lines to ensure correct acceptance of data at the right destination.

8.1 Main Feature Summary

Maximum number of devices	15
Maximum bus length	20 meters or 2 meters per device, whichever is less
Connection	star or chain Note that more than half of any connected devices must be powered up, even if they will not be used.
Data lines	8 DIO 1 to 8
Handshake lines	DAV Data available NRFD Not ready for data NDAC No data accepted
Bus management lines	EOI End or identity IFC Interface clear SRQ Service request ATN Attention REN Remote enable
Active level	+0.4 V
Inactive level	+3.3 V
	Note that all signal lines are active-low, and that they are wire-OR'd to allow participation by all devices.

In addition, there are eight ground lines, making a total of 24 lines. A diagram of the connector is shown in Figure 8-1.

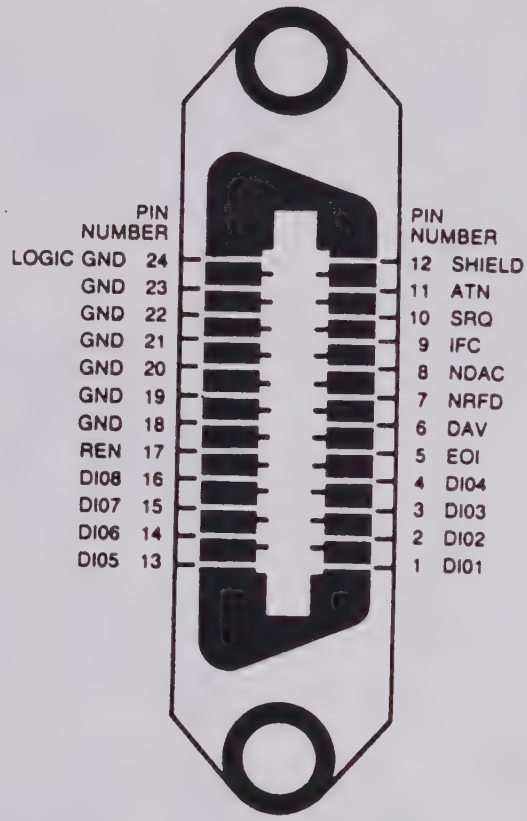

PIN NUMBER
LOGIC GND 24
GND 23
GND 22
GND 21
GND 20
GND 19
GND 18
REN 17
DI08 16
DI07 15
DI06 14
DI05 13
PIN NUMBER
12 SHIELD
11 ATN
10 SRQ
9 IFC
8 NDAC
7 NRFD
6 DAV
5 EOI
4 DI04
3 DI03
2 DI02
1 DI01

Figure 8-1

8.2 Functions in the GPIB

In order to allow satisfactory interconnection of several devices the following functions must be provided:

- Enabling any device to transmit data
- Preventing any device from transmitting data
- Enabling any device to receive data
- Preventing any device from receiving data
- Transmitting data to a specific device
- Ensuring that only one device is transmit
- Ensuring that transmitting takes place only when reception is possible
- Enabling any device to request servicing
- Identify type of data to be sent

Any device can be activated into the "talk" or "listen" state, and can be de-activated by the commands "untalk" and "unlisten". Also a device can be a "controller".

Maximum number of current talkers	1
Maximum number of current listeners	14
Maximum number of current controllers	1

8.3 Function of bus lines:

- DAV Data Available; talker says the data on the lines are valid.

- NRFD Not Ready For Data; listener says it is not ready for more data. All listeners must release the NRFD line, i.e., let it go high, before talker can send.

- NDAC No Data Accepted; listener says it has not yet accepted the data. Talker must hold all data lines steady until all listeners have released this line, i.e., it goes high.

Clearly the NRFD and NDAC are easy to implement by a wire-OR system, so that any one device asserting the signal prevents progress to the next step. Progress is made at the speed of the slowest listener. A simple timing diagram is given (Figure 8-2).

The bus management lines function as follows:

- EOI End Or Identify; talker sends this with last byte of a block transfer to indicate last byte. Also used with ATN to parallel poll devices for their Status Bit.

- IFC InterFace Clear; places the GPIB system into a quiescent state.

- SRQ Service ReQuest; any device can send it to the controller to indicate need for attention, and to request interruption of current operations.

- ATN ATteNtion; controller sends this to specify whether DIO lines are to be used for interface messages, e.g., addressing, or for data.

- REN Remote ENable; selects a device as being under local or remote control.

Addressing of the devices on the GPIB bus is made by a switch which can select values from 0 to 30.

For more detailed information on the GPIB bus consult the GPIB-IEEE488 document, ANSI/IEEE Std 488-1978.

IEEE Standards Office
Institute of Electrical and Electronic Engineers, Inc.
345 East 47th Street
New York, New York 10017

The principles of GPIB are quite simple - the system must wait for all users, and lines are wire OR'd so that all can pull the lines down.

The handshake sequence is illustrated in Figure 8-2 where the signal waveforms are sketched.

Figure 8-3 is a table listing the ASCII and IEEE-488 (GPIB) Code Chart.

APPENDIX A

Dec	Hex	ASCI char	IBM-PC char	IEEE-488 Multiline Interface Message (Sent with Attention true)
0	00	NUL		
1	01	SOH	^A	GTL - Go To Local
2	02	STX	^B	
3	03	ETX	^C	
4	04	EOT	^D	SDC - Selected Device Clear
5	05	ENQ	^E	PPC - Parallel Poll Configure
6	06	ACK	^F	
7	07	BEL		
8	08	BS		GET - Group Execute Trigger
9	09	HT		TCT - Take Control
10	0A	LF		
11	0B	VT		
12	0C	FF		
13	0D	CR		
14	0E	SO	^N	
15	0F	SI	^O	
16	10	DLE	^P	
17	11	DC1	^Q	LLO - Local Lock Out
18	12	DC2	^R	
19	13	DC3	^S	
20	14	DC4	^T	DCL - Device Clear
21	15	NAK	^U	PPU - Parallel Poll Unconfigure
22	16	SYN	^V	
23	17	ETB	^W	
24	18	CAN	^X	SPE - Serial Poll Enable
25	19	EM	^Y	SPD - Serial Poll Disable
26	1A	SUB		
27	1B	ESC	^[	
28	1C	FS	^\	
29	1D	GS	^]	
30	1E	RS	^^	
31	1F	US	^_	
32	20	SP		MLA - My Listen Address (listen 0)
33	21	!	!	MLA - My Listen Address (listen 1)
34	22	"	"	MLA - My Listen Address (listen 2)
35	23	#	#	MLA - My Listen Address (listen 3)
36	24	$	$	MLA - My Listen Address (listen 4)
37	25	%	%	MLA - My Listen Address (listen 5)
38	26	&	&	MLA - My Listen Address (listen 6)
39	27	'	'	MLA - My Listen Address (listen 7)
40	28	(	(	MLA - My Listen Address (listen 8)
41	29	)	)	MLA - My Listen Address (listen 9)
42	2A	*	*	MLA - My Listen Address (listen 10)
43	2B	+	+	MLA - My Listen Address (listen 11)
44	2C	,	,	MLA - My Listen Address (listen 12)
45	2D	-	-	MLA - My Listen Address (listen 13)

Dec	Hex	ASCII char	IBM-PC char	IEEE-488 Multiline Interface Message (Sent with Attention true)
46	2E	.	.	MLA - My Listen Address (listen 14)
47	2F	/	/	MLA - My Listen Address (listen 15)
48	30	0	0	MLA - My Listen Address (listen 16)
49	31	1	1	MLA - My Listen Address (listen 17)
50	32	2	2	MLA - My Listen Address (listen 18)
51	33	3	3	MLA - My Listen Address (listen 19)
52	34	4	4	MLA - My Listen Address (listen 20)
53	35	5	5	MLA - My Listen Address (listen 21)
54	36	6	6	MLA - My Listen Address (listen 22)
55	37	7	7	MLA - My Listen Address (listen 23)
56	38	8	8	MLA - My Listen Address (listen 24)
57	39	9	9	MLA - My Listen Address (listen 25)
58	3A	:	:	MLA - My Listen Address (listen 26)
59	3B	;	;	MLA - My Listen Address (listen 27)
60	3C	<	<	MLA - My Listen Address (listen 28)
61	3D	=	=	MLA - My Listen Address (listen 29)
62	3E	>	>	MLA - My Listen Address (listen 30)
63	3F	?	?	UNL - Unlisten
64	40	@	@	MTA - My Talk Address (talk 0)
65	41	A	A	MTA - My Talk Address (talk 1)
66	42	B	B	MTA - My Talk Address (talk 2)
67	43	C	C	MTA - My Talk Address (talk 3)
68	44	D	D	MTA - My Talk Address (talk 4)
69	45	E	E	MTA - My Talk Address (talk 5)
70	46	F	F	MTA - My Talk Address (talk 6)
71	47	G	G	MTA - My Talk Address (talk 7)
72	48	H	H	MTA - My Talk Address (talk 8)
73	49	I	I	MTA - My Talk Address (talk 9)
74	4A	J	J	MTA - My Talk Address (talk 10)
75	4B	K	K	MTA - My Talk Address (talk 11)
76	4C	L	L	MTA - My Talk Address (talk 12)
77	4D	M	M	MTA - My Talk Address (talk 13)
78	4E	N	N	MTA - My Talk Address (talk 14)
79	4F	O	O	MTA - My Talk Address (talk 15)
80	50	P	P	MTA - My Talk Address (talk 16)
81	51	Q	Q	MTA - My Talk Address (talk 17)
82	52	R	R	MTA - My Talk Address (talk 18)
83	53	S	S	MTA - My Talk Address (talk 19)
84	54	T	T	MTA - My Talk Address (talk 20)
85	55	U	U	MTA - My Talk Address (talk 21)
86	56	V	V	MTA - My Talk Address (talk 22)
87	57	W	W	MTA - My Talk Address (talk 23)
88	58	X	X	MTA - My Talk Address (talk 24)
89	59	Y	Y	MTA - My Talk Address (talk 25)
90	5A	Z	Z	MTA - My Talk Address (talk 26)
91	5B	[	[	MTA - My Talk Address (talk 27)
92	5C	\	\	MTA - My Talk Address (talk 28)

Dec	Hex	ASCII char	IBM-PC char	IEEE-488 Multiline Interface Message (Sent with Attention true)
93	5D	]	]	MTA - My Talk Address (talk 29)
94	5E	^	^	MTA - My Talk Address (talk 30)
95	5F	_	_	UNT - Untalk
96	60	`	`	
97	61	a	a	
98	62	b	b	
99	63	c	c	
100	64	d	d	
101	65	e	e	
102	66	f	f	
103	67	g	g	
104	68	h	h	
105	69	i	i	
106	6A	j	j	
107	6B	k	k	
108	6C	l	l	
109	6D	m	m	
110	6E	n	n	
111	6F	o	o	
112	70	p	p	
113	71	q	q	
114	72	r	r	
115	73	s	s	
116	74	t	t	
117	75	u	u	
118	76	v	v	
119	77	w	w	
120	78	x	x	
121	79	y	y	
122	7A	z	z	
123	7B	{	{	
124	7C	|	|	
125	7D	}	}	
126	7E	~	~	
127	7F	NUL		
128	80		Ç	
129	81		ü	
130	82		é	
131	83		â	
132	84		ä	
133	85		à	
134	86		å	
135	87		ç	
136	88		ê	
137	89		ë	
138	8A		è	
139	8B		ï	

Dec	Hex	ASCII char	IBM-PC char	IEEE-488 Multiline Interface Message (Sent with Attention true)
140	8C		î	
141	8D		ì	
142	8E		Ä	
143	8F		Å	
144	90		É	
145	91		æ	
146	92		Æ	
147	93		ô	
148	94		ö	
149	95		ò	
150	96		û	
151	97		ù	
152	98			
153	99		Ö	
154	9A		Ü	
155	9B		¢	
156	9C		£	
157	9D		¥	
158	9E		₧	
159	9F		ƒ	
160	A0		á	
161	A1		í	
162	A2		ó	
163	A3		ú	
164	A4		ñ	
165	A5		Ñ	
166	A6		ª	
167	A7		º	
168	A8		¿	
169	A9		⌐	
170	AA		¬	
171	AB		½	
172	AC		¼	
173	AD		¡	
174	AE		«	
175	AF		»	
176	B0			
177	B1		▒	
178	B2		▓	
179	B3		│	
180	B4		┤	
181	B5		╡	
182	B6		╢	
183	B7		╖	
184	B8		╕	
185	B9		╣	
186	BA		║	
187	BB		╗	

Dec	Hex	ASCII char	IBM-PC char	IEEE-488 Multiline Interface Message (Sent with Attention true)
188	BC		╝	
189	BD		╜	
190	BE		╛	
191	BF		┐	
192	C0		└	
193	C1		┴	
194	C2		┬	
195	C3		├	
196	C4		─	
197	C5		┼	
198	C6		╞	
199	C7		╟	
200	C8		╚	
201	C9		╔	
202	CA		╩	
203	CB		╦	
204	CC		╠	
205	CD		═	
206	CE		╬	
207	CF		╧	
208	D0		╨	
209	D1		╤	
210	D2		╥	
211	D3		╙	
212	D4		╘	
213	D5		╒	
214	D6		╓	
215	D7		╫	
216	D8		╪	
217	D9		┘	
218	DA		┌	
219	DB		▉	
220	DC		▌	
221	DD		▐	
222	DE		▀	
223	DF			
224	E0		α	
225	E1		ß	
226	E2		Γ	
227	E3		π	
228	E4		Σ	
229	E5		σ	
230	E6		µ	
231	E7		τ	
232	E8		Φ	
233	E9			
234	EA		Ω	

Dec	Hex	ASCII char	IBM-PC char	IEEE-488 Multiline Interface Message (Sent with Attention true)
235	EB		δ	
236	EC		∞	
237	ED		ϕ	
238	EE		ϵ	
239	EF		∩	
240	F0		≡	
241	F1		±	
242	F2		≥	
243	F3		≤	
244	F4		⌠	
245	F5		⌡	
246	F6		÷	
247	F7		≈	
248	F8		°	
249	F9		•	
250	FA		·	
251	FB		√	
252	FC		η	
253	FD		²	
254	FE		■	
255	FF			

APPENDIX B
9100 Series Trigger Modes

I) **Selection of a Test Waveform** - The following criteria should be considered in selecting a waveform to use in trigger mode testing:

A) Length - The minimum length for a waveform to be generated in any triggering mode other than continuous is 72 points. Waveforms considerably longer than 72 points should also be avoided, since it becomes increasingly difficult to determine if the proper number of points have been generated with longer waveforms.

B) The first and last points of the waveform to be used should be known, and different from one another, so that one can tell if the waveform starts and ends at the proper points.

C) The step amplitude between adjacent points of the waveform should be discernibly large.

D) A dual channel wave is preferable to a single channel wave, simply because it also proves that some other important features of the device are functional.

If you do not happen to have a waveshape stored in your unit that meets the criteria above, one can easily be created using Easywave software. The waveform data below can be entered in Array Editing mode in Easywave® .

Channel 1:

	0	1	2	3	4	5	6	7	8	9
0	146	182	219	255	0	36	73	109	146	182
1	219	255	0	36	73	109	146	182	219	255
2	0	36	73	109	146	182	219	255	0	36
3	73	109	146	182	219	255	0	36	73	109
4	END									

Channel 2:

	0	1	2	3	4	5	6	7	8	9
0	109	73	36	0	255	219	182	146	109	73
1	36	0	255	219	182	146	109	73	36	0
2	255	219	182	146	109	73	36	0	255	219
3	182	146	109	73	36	0	255	219	182	146
4	END									

When passed to the AFG and generated, the data above should produce the waveform shown in Fig. B-1. We will call this

waveform trigtest.wad. Create this waveform and download it to your AFG if you wish, and then load it, or another waveshape that meets the above criteria, into high-speed memory, responding with 1 when asked for the number of repetitions. Also, change the clock rate to 10 MHz, to make the output risetimes ignorably small with respect to the clock period.

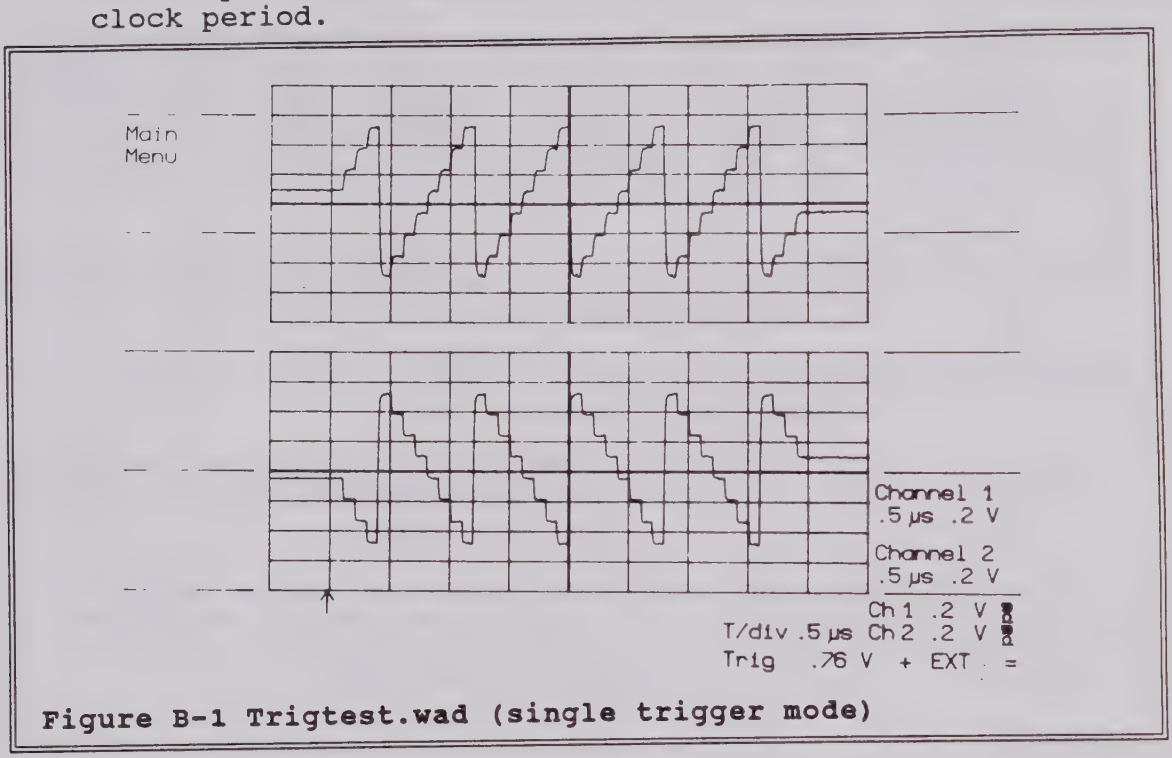


Figure B-1 Trigtest.wad (single trigger mode)

II) Continuous Mode

A) Analog Outputs - In continuous mode, it is virtually impossible to distinguish the points at which most waveforms begin and end, because the generator automatically returns to the first point after the last point, without interruption. Our trigtest waveform, in continuous mode, would therefore look like a never-ending series of 8-point ramps, as shown in Fig. B-2A.

B) Timing Outputs -

1) Clock Outputs - The 2 rear panel clock outputs should appear identical in continuous mode, both running cw at the timebase rate (twice the clock rate when generating dual channel waveforms. The output levels should be 0 mV in the high state, and -800 mV in the low state when driving a 50 Ω load. The Clock 2 output in continuous mode is shown as the lower trace in Fig. B-2B.

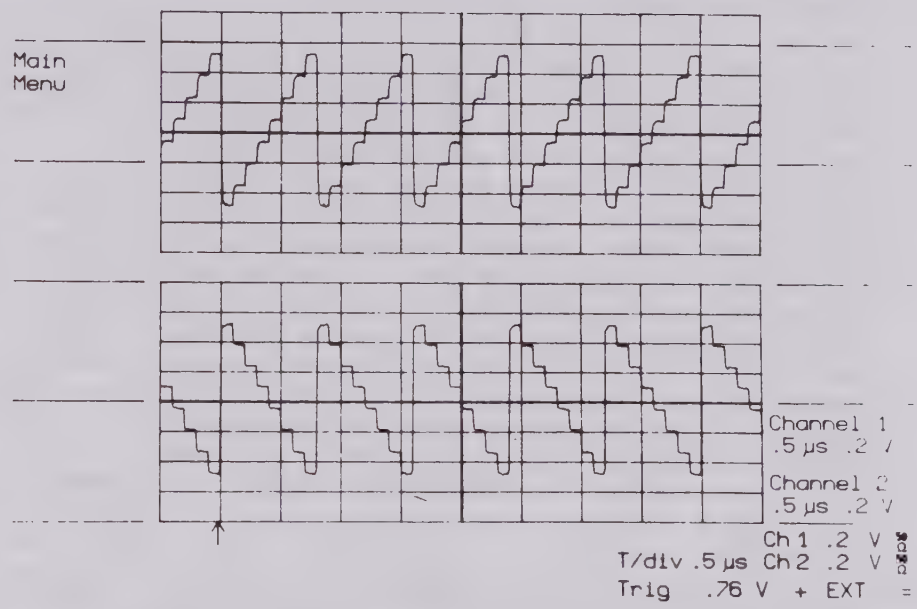


Figure B-2A Trigtest.wad (continuous trigger mode)

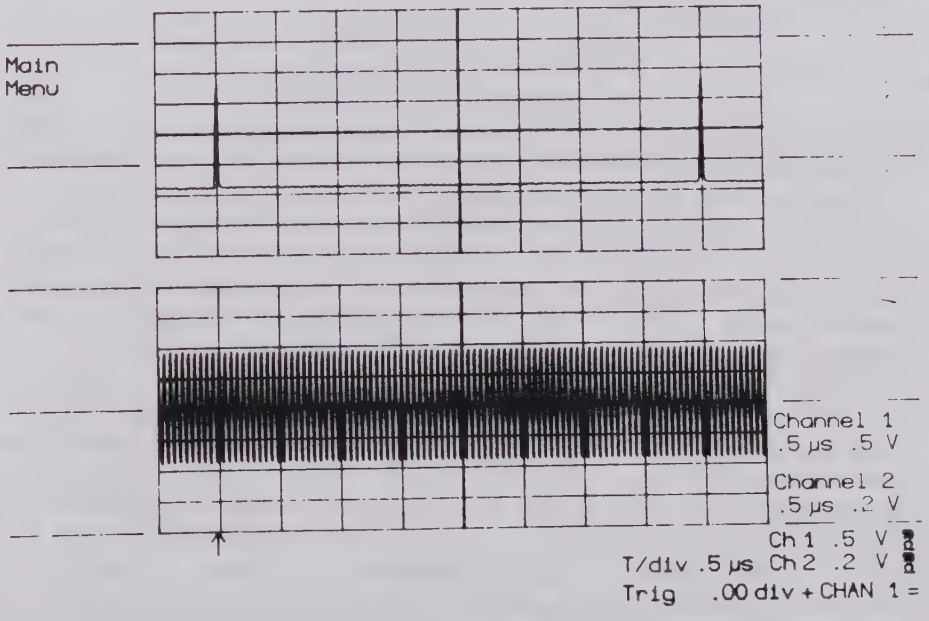


Figure B-2B START and CLK2 outputs for trigtest.wad in continuous mode

2) Sync Output - The sync output is not available in continuous mode.

3) Start Output - The start output is the only one of the three front panel timing outputs available in continuous mode. It is intended mainly for use as an oscilloscope trigger or similar applications, and occurs a few points before the actual start of the waveform. How many points before the first point of the waveform the start pulse occurs is dependant on the length of the waveform and the clock rate. For waveforms greater than 72 points long, and at clock rates below 20 MHz, the start pulse will occur 8 points before the start of the waveform. Due to certain asynchronous delays in the path of the start pulse, as the clock rate increases, the start pulse seems to occur closer to the first point of the waveform. For waveforms of less than 72 points, the start pulse may appear to occur anywhere from 2 to 8 points before the first point of the waveform, depending again on the clock rate and the actual waveform length. The start output in continuous mode is shown as the upper trace in Fig. B-2B. Its amplitude is greater than 1.5 V into 50 Ω (TTL level into a high impedance) and the pulse should be about 25 nsec wide.

4) Marker Output - The marker output is not available in continuous mode.

III) Single Mode

A) Analog Outputs - In single trigger mode, the waveform is output one time each time a trigger is recognized. Before a trigger can be recognized, however, the trigger circuitry must be armed. In the 9100 Series, trigger arming can be automatic, (arm source auto) occurring immediately after the waveform reaches completion, or done only upon command (arm source bus). Arming the trigger circuitry causes the output to go to the first point of the waveform.

The AFG's single trigger mode analog outputs will therefore look subtly different depending on the arm source. If the arm source is bus, the last visible transition on any given waveform will be from the next-to-last point to the last point. If auto-arming is enabled, an additional transition will occur about 10 timebase cycles (i.e., 10 single channel points or 5 points for dual channel waves) after the above mentioned one, from the last point to the first. Fig. B-3, shows trigtest.wad in single mode with the bus selected as arm source (a), and with auto arming enabled (b).

Figure B-3A Trigtest.wad (single trigger mode, arm source bus)

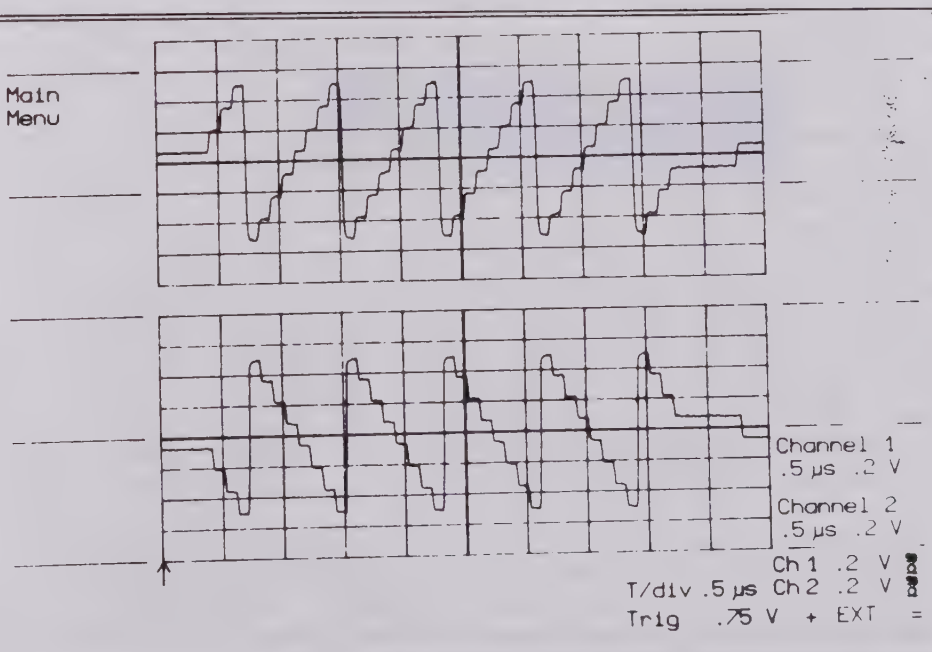


Figure B-3B Trigtest.wad (single trigger mode, arm source auto

B) Timing Outputs

1) Clock Outputs - The clock 1 output looks the same for any triggering mode. It runs cw at the internal timebase rate and is active whether or not a waveform is being generated. The clock 2 output resembles the compliment of the signal that drives the internal clock driver stage on the 9100-6 card. This output will only have a signal on it while waveforms are being output. Its quiescent state is low if the AFG's trigger is armed, but high if the unit is not armed. Note that in the upper trace of Fig. B-4A, the clock 2 output starts in the low state, because the AFG must be armed before responding to a trigger, but stops in the high state, and remains there until an arm command is received. Conversely, in Fig. B-4B, while the clock still starts in the low state, it remains in the high state only for the time required for auto arming to occur, and then goes low. The astute observer might also note that during its active period this clock output is running at twice the point output rate. This is again because the timebase rate is twice the point output rate for dual channel waveforms.

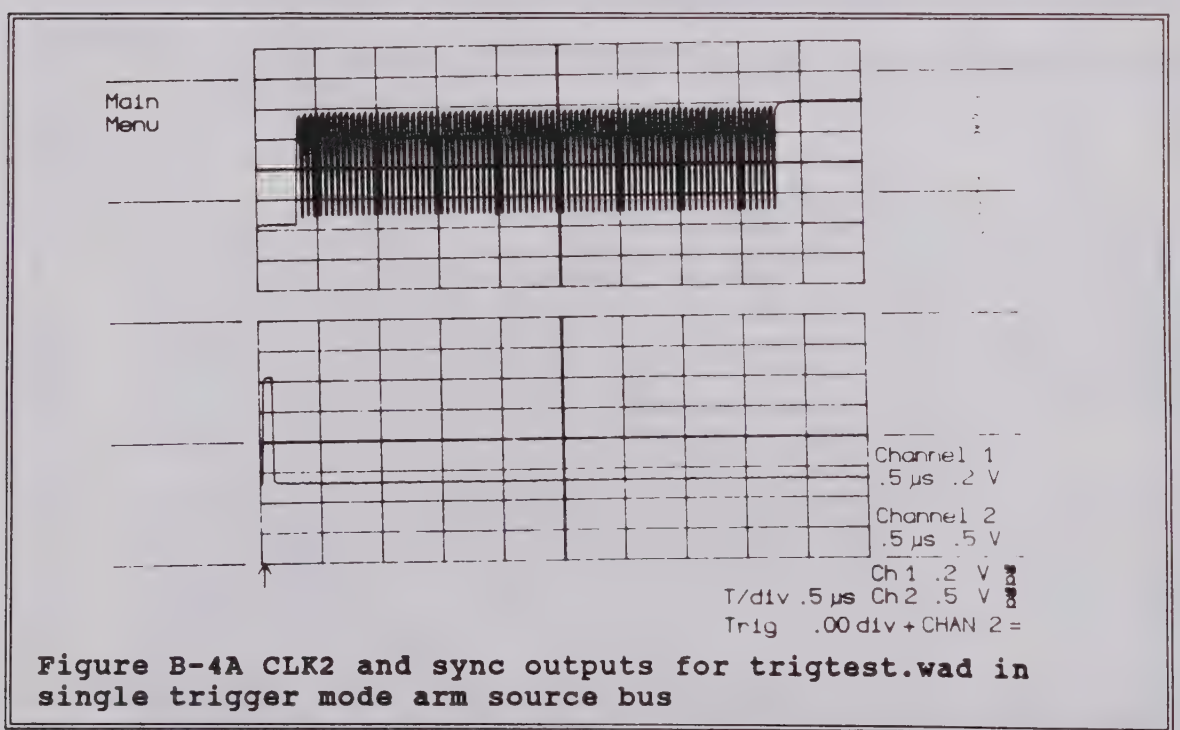


Figure B-4A CLK2 and sync outputs for trigtest.wad in single trigger mode arm source bus

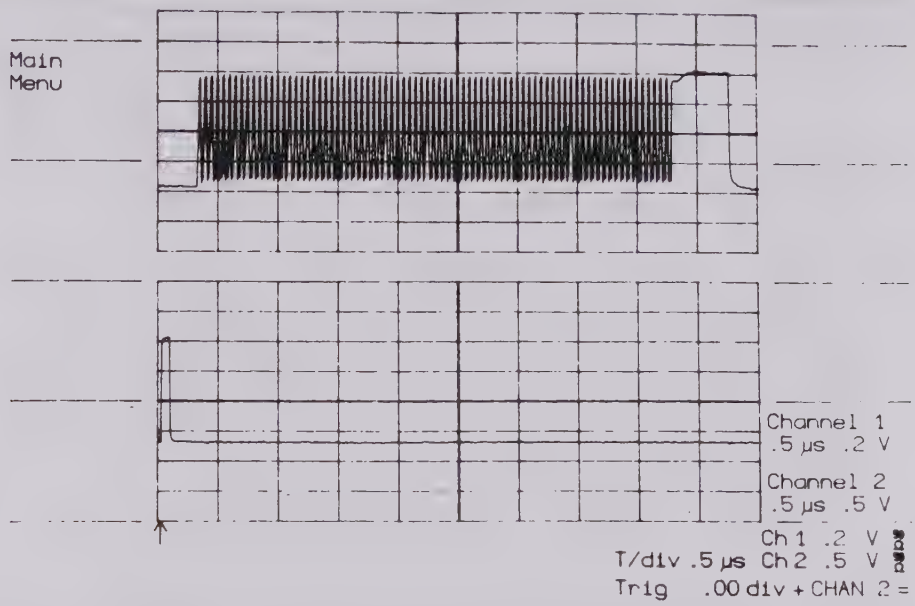


Figure B-4B CLK2 and sync outputs for trigtest.wad in single trigger mode arm source auto

2) Sync Output - The sync output in single trigger mode is the earliest in time of the three front panel user timing outputs, occurring 2 timebase cycles after the trigger that commences the waveform generation process is latched. It should be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 and 100 nsec. wide. In single trigger mode, 1 sync pulse will occur for every trigger received, regardless of the source of the triggering signal or the arming source. The sync output for a single trigger mode output cycle of trigtest.wad is shown as the lower trace in Figs. X-4A and B. Note that the sync output was used as the oscilloscope trigger for this and all other Figs. in this chapter, except for the continuous mode Figs., for which the start output was used.

3) Start Output - The start pulse occurs a programmed number of timebase cycles after the latching of the triggering signal, coincident with the start of the clock 2 output and the first transition of the analog outputs. It should be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 & 100 nSec. wide. The minimum delay from the latching of a trigger to the start output (and the start of the clock 2 and analog outputs) in single mode is 4

timebase cycles. Thus the default value for trigger delay is 4 points. Note that for a dual channel mode output, 4 points is 8 timebase cycles, so the default value for dual channel trigger delay is not the minimum, which is 2. This output is also unaffected by the source of the arming signal. The start output for trigtest.wad using the default trigger delay of 4 points is shown as the upper trace of Fig. B-5.

4) Marker Output - The marker output occurs a programmed number of timebase cycles after the latching of the triggering signal. It should be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 and 100 nsec. The discussion of default and minimum values for trigger delay in the start output section above also applies to the marker delay. Note that the marker delay (as well as the trigger delay) is measured from the latching of the triggering signal, NOT from the start of the waveform. Thus, to place the marker at the 20th pair of points of the trigtest.wad output, as shown in the lower trace of Fig. B-5, the marker delay is programmed for 24 points (i.e., 20 points more than the 4 point minimum). Note that, due to the segment repetition and linking capabilities of the 9100 family, there is no way for the software to know how long a given waveform is. Therefore, if an attempt is made to place the marker past the end of the waveform, no error message will be returned, but no marker output will occur. Also note that the trigger delay and marker delay counters are independent of one another, and must be programmed individually. If trigger delay is increased and it is desired to keep the marker in the same relative position on the waveform, the marker delay must be increased by the same amount.

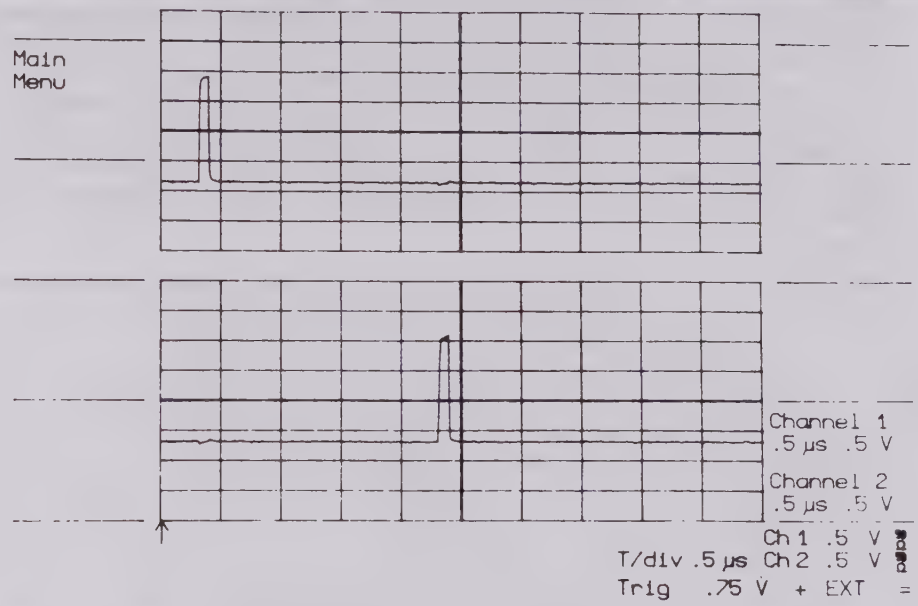


Figure B-5 START and MARKER outputs for trigtest.wad in single trigger mode

IV) Burst Mode

A) Analog Outputs - In burst mode, the waveform is output a programmed number of times (up to 65,535), each time a trigger is recognized. Single mode is actually a special case of burst mode, with the programmed number being 1. Everything discussed under single mode about arm sources and how the waveform ends applies to burst mode also. Shown in Fig. B-6, are the analog outputs for trigtest.wad in burst mode, auto armed, with 2 repetitions of the waveform.

B) Timing Outputs - The timing outputs in burst mode will be identical to those in single mode with the following exceptions:

1) Clock 2 Output - The clock will be active for twice as long as in Fig. B-4A and B, because twice as many points are output if the waveform repeats twice. The final state of this output will again depend on the source of the arming signal.

2) The Sync, Start and Marker outputs will occur only once, i.e., there will not be separate User Timing outputs for the second repetition. Recall that these outputs occur

at a fixed time following the latching of the trigger, and that no trigger is required to produce the subsequent repetitions in burst mode. The marker pulse will still occur coincident with the 20th pair of points of the trigtest.wad analog output in burst mode with 2 repetitions, but the 20th point is no longer at the center of the output signal. The pulses should all be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 and 100 nsec wide.

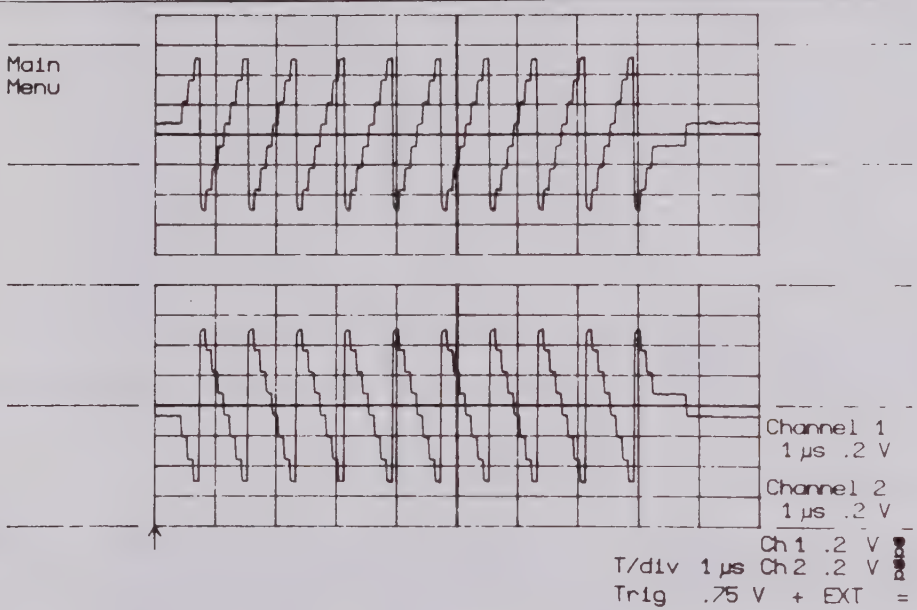


Figure B-6 Trigtest.wad (trigger mode BURST, 2 arm source auto)

V) Recurrent Mode

A) In recurrent mode, the waveform is generated a programmed number of times (again, up to 65,535). The AFG then stops, re-arms and re-triggers itself. After a programmable trigger delay of up to a million points, the cycle repeats. Generation repeats in this manner (delay, output, re-arm, re-trigger, delay, output...) indefinitely, until aborted. The recurrent mode analog output for trigtest.wad with 1 repetition is shown in Fig. B-7.

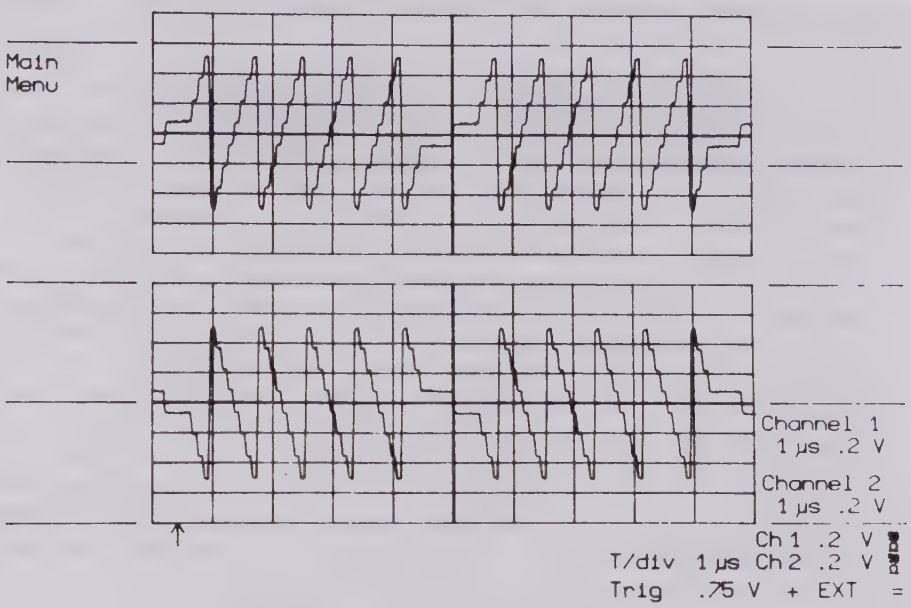


Figure B-7 Trigtest.wad (trigger mode Recurrent, 1)

B) Timing Outputs

1) Clock 2 Output - In recurrent mode, the clock 2 output runs at the timebase rate (twice the point output rate for dual channel waveform outputs) during the interval when waveform points are in transition. The clock output stops in the high state & remains there while re-arming occurs, after which it returns to the low state. It remains low during the trigger delay period (the minimum of 8 points, by default, in our example) and then starts up again at the timebase rate. This cycle of events also repeats until aborted. The clock 2 output for trigtest.wad in recurrent mode with 1 repetition and default trigger delay is shown in the upper trace of Fig. B-8.

2) Sync Output - In recurrent mode, a sync output will occur each time the generator re-triggers itself, but not for the individual repetitions of the waveshape between re-triggers. It should be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 and 100 nsec. wide. The sync output for trig-test.wad in recurrent mode with 1 repetition and default trigger delay is shown in the lower trace of Fig. B-8. If the repetition count were

2, there would still be only 2 sync pulses shown, with the second occurring about 4 μSec. later than in Fig. B-8.

3) Start Output - As in single and burst modes, the start output occurs a programmed number of timebase cycles after the triggering (or in this case, re-triggering) signal is latched. It should be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 and 100 nsec. wide. For the sake of ease of reference, however, trigger delay is defined slightly differently in recurrent mode, because the user really has no idea when the re-triggering signal happens. We define trigger delay in recurrent mode as the time between the end of one series of repetitions and the beginning of the next. By that definition, the minimum trigger delay in recurrent mode is 16 timebase cycles, or 8 dual channel points. The default position of the start pulse for trigtest.wad would therefore be 8 point periods after the end of the preceding series.

   The only point that may still be unclear is exactly where a waveform can be said to begin and end. We define the end of a waveform to occur 1 clock period after the transition from the next-to-last point to the last point, and the beginning of a waveform to be 1 clock period before the transition from the first point to the second. The upper trace of Fig. B-9 shows channel 1's analog output for the last part of 1 recurrent series of trigtest.wad, and the first part of the next series, at an expanded time scale. The lower trace shows the position of the start pulse relative to the analog output. The lower trace of Fig. B-9 is START output. The cursors show where the ending and starting points are defined. As you can see, the time difference is indeed 8 point periods at 10 MHz. The upper trace of Fig. B-10, shows the start pulse's position at the same time scale as Figs. B-7 and B-8.

4) Marker Output - The marker delay is also measured from the end of the previous series. It should be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 and 100 nsec. wide. It likewise defaults to 16 timebase cycles, or 8 dual channel points. To position the marker at the 20th pair of points in trigtest.wad, as shown in Fig. B-10, the marker delay is programmed for 28 points.

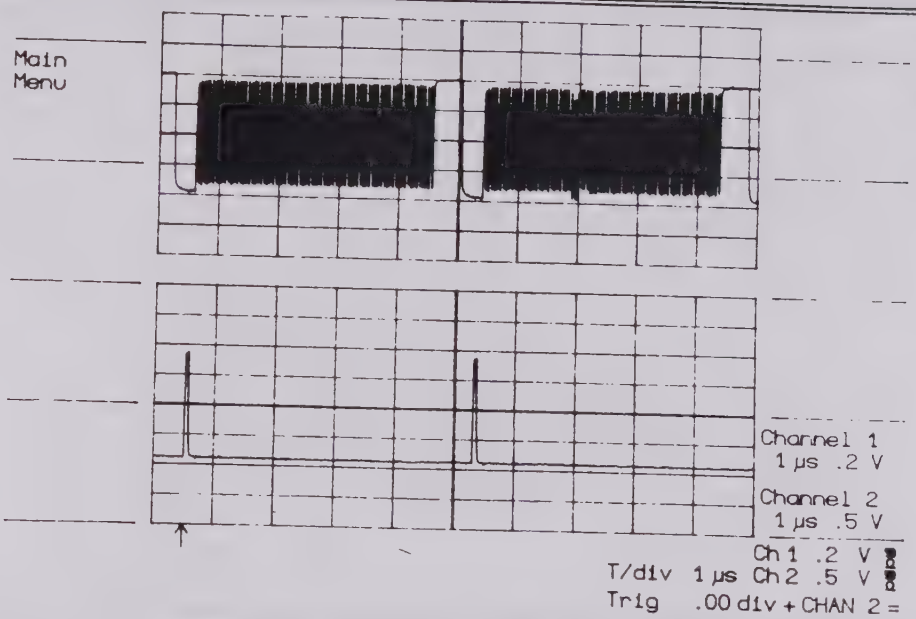


Figure B-8 CLK2 and SYNC for trigtest.wad (trigger mode Recurrent

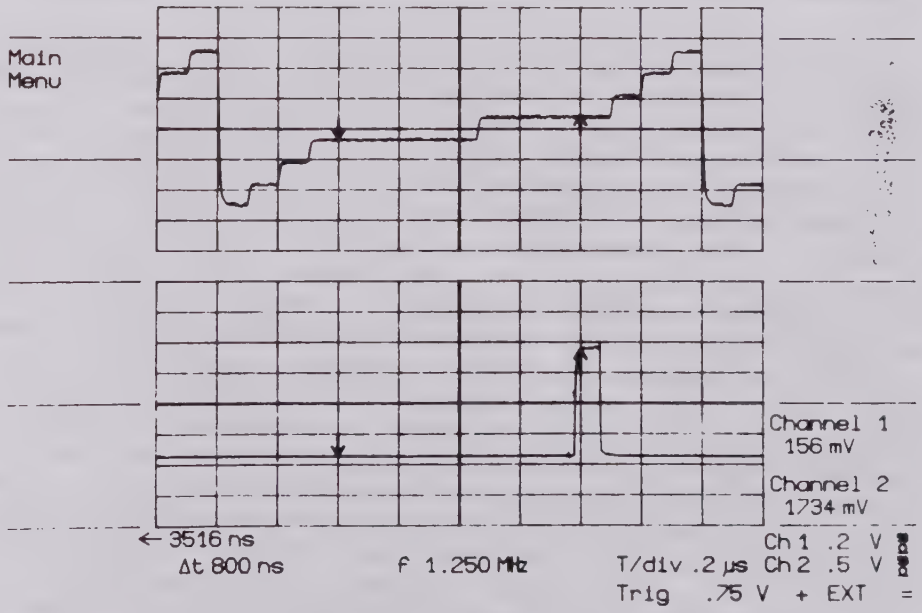


Figure B-9 CH1 and START expanded view for trigtest.wad (trigger mode Recurrent)

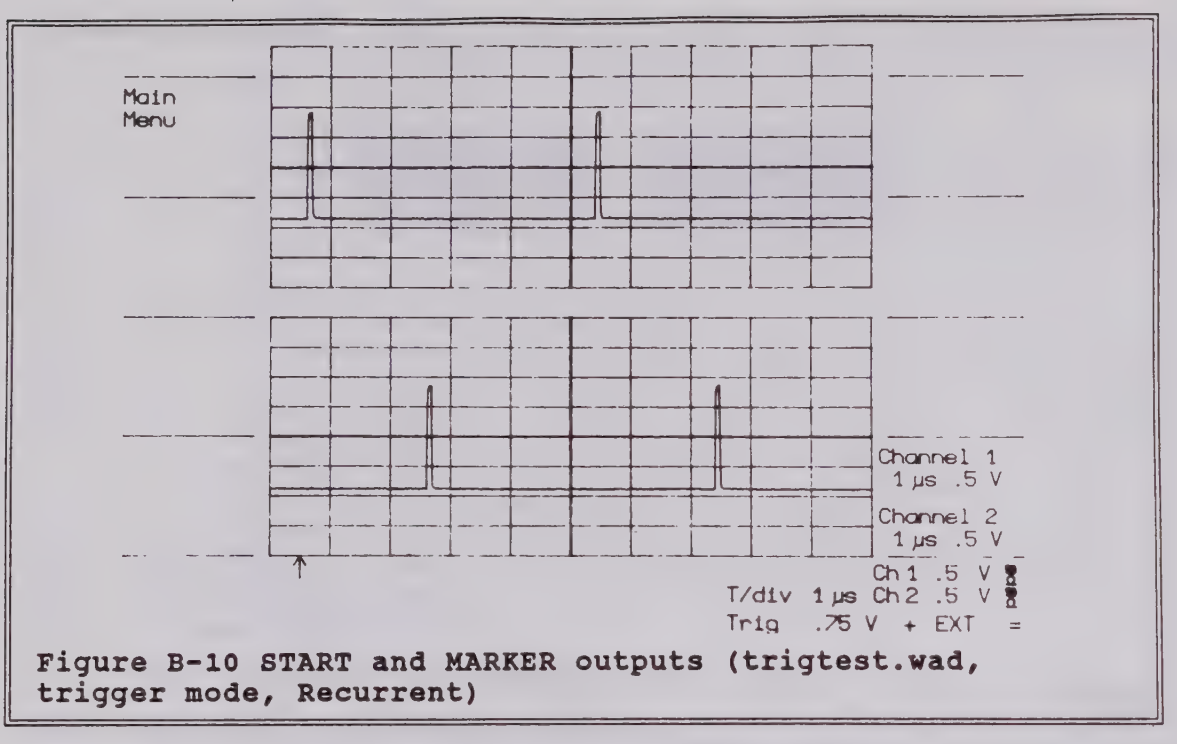


Figure B-10 START and MARKER outputs (trigtest.wad, trigger mode, Recurrent)

VI) Gate Mode

A) Analog Outputs - Gated operation in the 9100 family is accomplished in the following manner. The leading edge of the gate signal is latched like any other triggering signal. Once this event is latched, the generator operates as it would in continuous mode until the trailing edge of the gate signal. When the "closing" of the gate is detected, the generator completes the waveform it is currently generating (i.e. continues until the last point of the present waveform), stops, re-arms itself and awaits the next "opening" of the gate. The number of times that a waveform repeats in gated mode is therefore totally a function of the gate width. Using trigtest.wad as an example, and remembering that the output occurs 4 point periods after the triggering signal is latched, we can determine that gate signals less than 4.4 µSec. wide will result in a single repetition of the waveform (which is 40 point pairs long at 100 nsec./point), gate signals between 4.4 and 8.4 µsec. will result in 2 repetitions, Gates between 8.4 and 12.4 µsec. will result in 3 repetitions, etc. The upper trace of Fig. B-11 shows channel 1's analog output when running trig- test.wad in gated mode, with the gate signal shown in the lower trace.

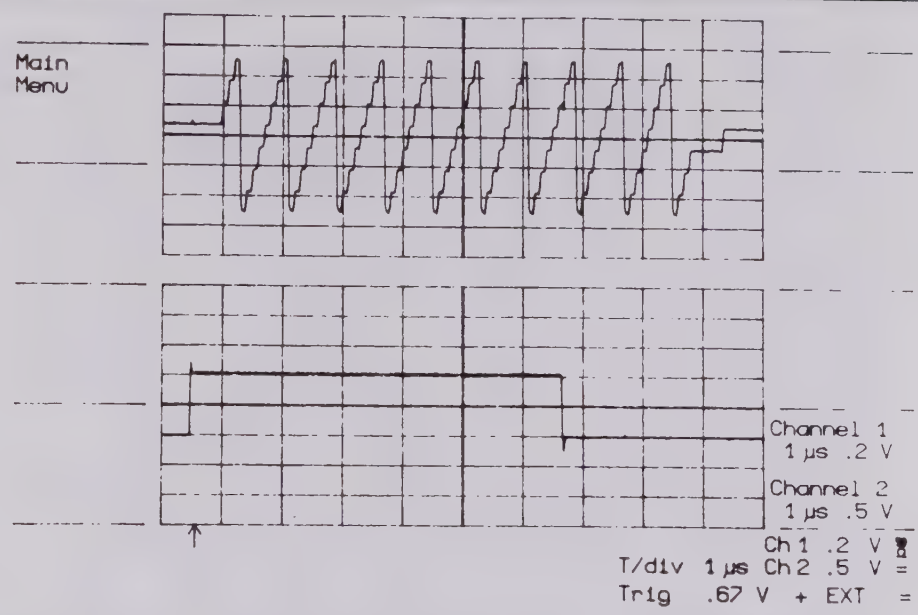


Figure B-11 CH1 output and GATE input (trigtest.wad, triggr mode, Gate)

B) Timing Outputs

1) Clock 2 Output - In gated mode, the clock 2 output will run at the timebase rate while the waveform is being output, stop in the high state when the waveform stops, and switch to the low state after the re-arming operation is completed. The clock output for trigtest.wad in gated mode is shown as the upper trace of Fig. B-12.

2) Sync Output - The sync output in gated mode will occur 2 timebase cycles after the leading edge of the gate is latched, and will occur only once per gate. Because of this, the sync pulse is a better choice for an oscilloscope trigger in gated mode than the start pulse, which may occur more often. It should be greater than 1.5 V in amplitude into a 50 Ω load (TTL level into a high impedance), and between 50 and 100 nsec. wide. The sync output for trigtest.wad in gated mode is shown as the lower trace in Fig. B-12. Note that the trigger delay may be varied in gate mode, to delay the AFG's response to the gate opening, and that the sync output will occur before the delay period.

3) Start Output - The start pulse in gated mode occurs once for each repetition of the waveform within the gate period. Its position, however, may not be quite what

one would intuitively expect, since it occurs at the end of each repetition. The explanation for this placement is as follows. As far as the start pulse circuitry is concerned, gate mode is the same as continuous mode. Note that the pulse width is only about 25 nsec. in this mode, as it is in continuous (the amplitude is still >1.5 V into 50 Ω or TTL level into a high-z). In continuous mode, the starting point of any given waveform repetition is identical to the ending point of the previous repetition. The 9100-6 card, which generates all these timing signals, receives lots of information to tell it when a waveform's end is approaching, because it is this card which must decide where and when to stop the output. It does not know, however, when a waveform is beginning. The only consequence of putting the start pulse at the end of a waveform repetition rather than at the beginning in continuous mode is that there is no start pulse for the very first output, which is quite trivial. We do see the effects of this placement in gated mode. As stated above, we recommend using the sync pulse for an oscilloscope trigger in gated mode. If an application should arise in which a pulse is needed for each repetition of the waveform within the gate, the sync and start pulses may be logically OR'd together with some external circuitry (remember that these outputs are capable of driving TTL loads). The start output for trigtest.wad in gated mode is shown as the upper trace in Fig. B-13.

4) Marker Output - The marker output will occur once per gate in gated mode, a programmed number of points after the latching of the leading edge of the gate. The marker output for trigtest.wad in gate mode is shown as the lower trace in Fig. B-13.

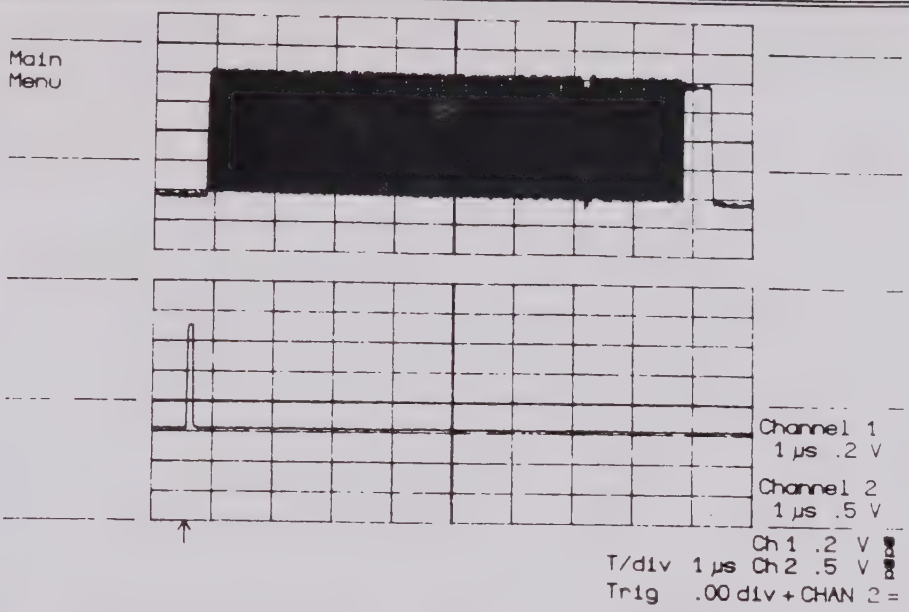


Figure B-12 CLK2 and SYNC outputs for trigtest.wad, trigger mode Gate

Figure B-13 START and MARKER outputs for trigtest.wad, trigger mode Gate

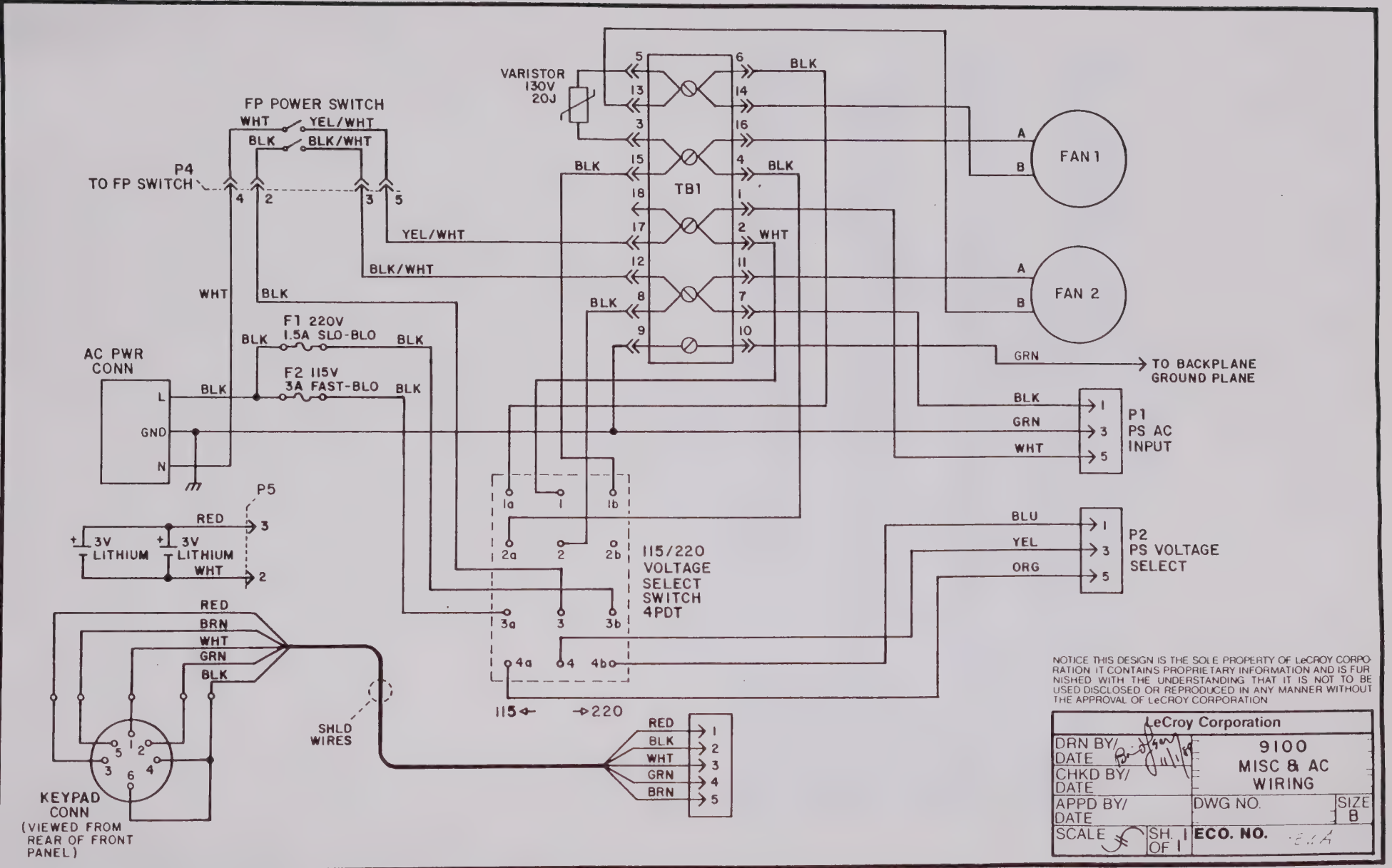
PLEASE NOTE

When production originally started for the 9100 family, the units were designed and shipped with the 9100-13 processor board and the 9100-3 Battery Backed Up Memory Board. The 9100-3 used a rechargable Ni-Cad battery.

About September of 1989, a new board known as the 9100-16 replaced the previous 9100-13 and 9100-3 combination. The battery type was changed to a non-rechargable Lithium type battery.

To provide as thorough a documentation package as possible, all schematics are included in this service manual even though your unit will not contain all of the board types documented.

The 9109 uses a 9100-22 board which develops the digital word outputs. This board is not used in the 9100 or 9101.



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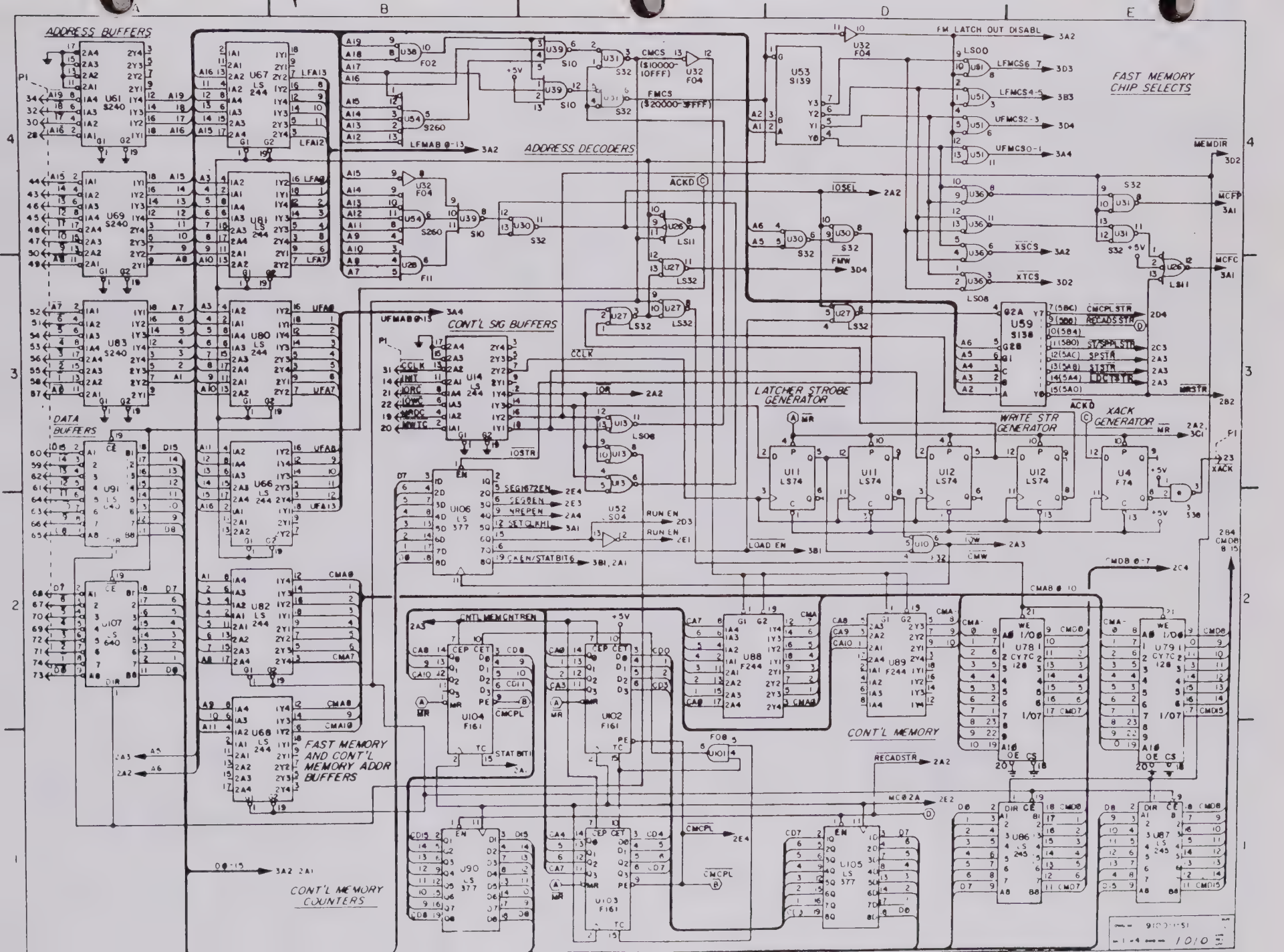
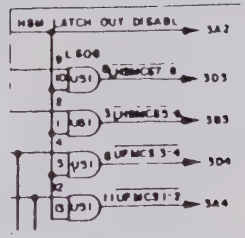
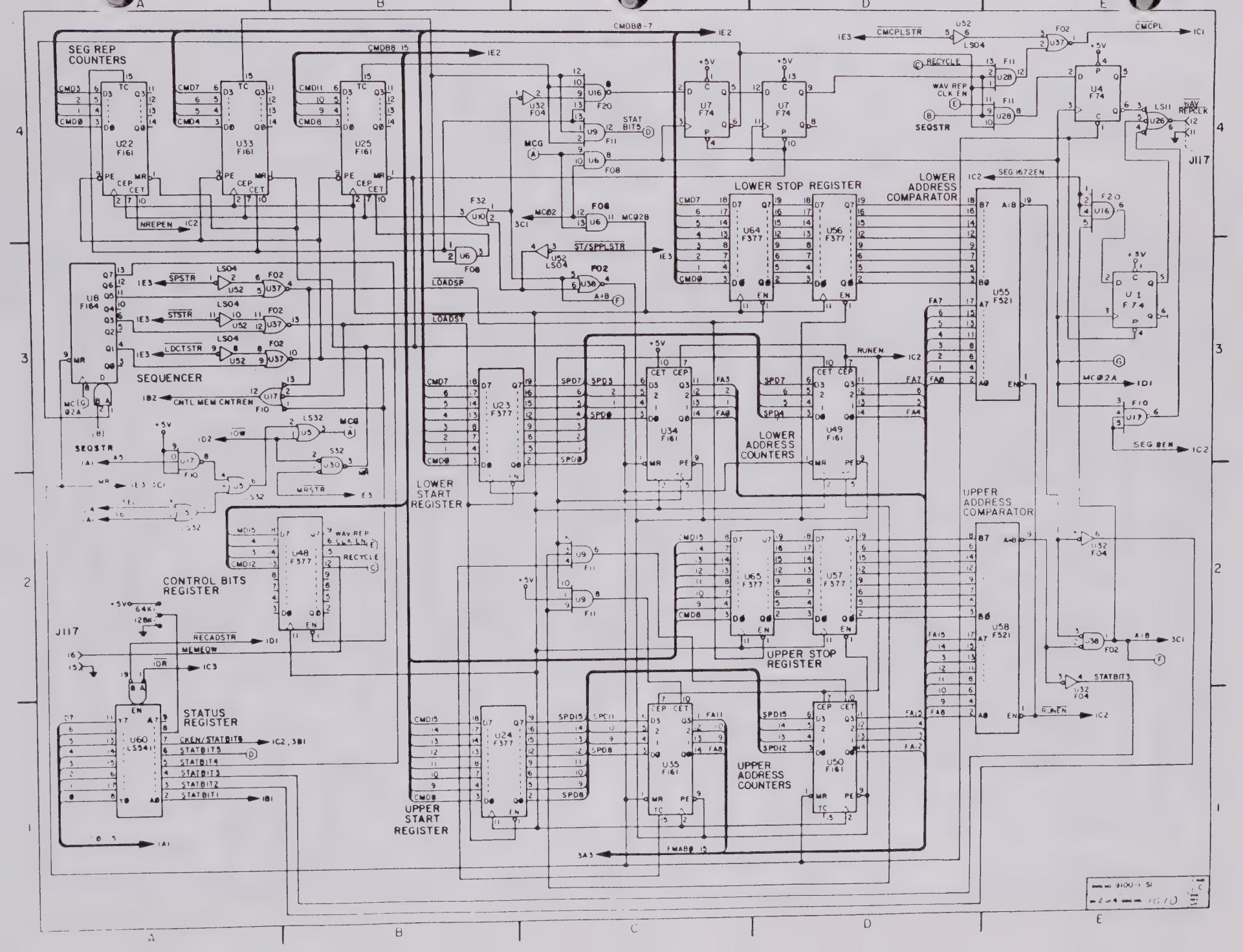
LeCroy Corporation			
DRN BY/ DATE		9100 MISC & AC WIRING	
CHKD BY/ DATE			
APPD BY/ DATE		DWG NO.	SIZE B
SCALE	SH. 1 OF 1	ECO. NO.	


ADDRESS BUFFERS
ADDRESS DECODERS
FAST MEMORY CHIP SELECTS
DATA BUFFERS
CONT'L SIG BUFFERS
LATCHER STROBE GENERATOR
WRITE STR GENERATOR
XACK GENERATOR
FAST MEMORY AND CONT'L MEMORY ADDR BUFFERS
CONT'L MEMORY
CONT'L MEMORY COUNTERS
FM LATCH OUT DISABL
LFMAB 0-13
LFMCS6
LFMCS4-5
UFMCS2-3
UFMCS0-1
XSCS
XTCS
IOSEL
FMW
ACKD
MEMDIR
MCFP
MCFC
MRSTR
XACK
CCLK
IOR
IOW
IOSTR
RUN EN
LOAD EN
CMW
CMDB 0-7
CMAB 0-10
RECADSTR
MCB2A
CMCPL
CNTL MEMCNTREN
DB 0-15
U61 S240
U67 LS 244
U53 S139
U32 F04
U59 S138
U11 LS74
U12 LS74
U4 F74
U106 LS 377
U104 F161
U102 F161
U103 F161
U88 F244
U89 F244
U78 1/0
U79 1/0
U86 LS 245
U87 LS 245
U90 LS 377
U105 LS 377



NOTE: THIS PAGE OF SCHEMATIC REFLECTS CONNECTIONS FOR REV. E
AND EARLIER 9100-1 BOARDS ONLY.


SEG REP COUNTERS
SEQUENCER
CONTROL BITS REGISTER
STATUS REGISTER
LOWER START REGISTER
UPPER START REGISTER
LOWER STOP REGISTER
UPPER STOP REGISTER
LOWER ADDRESS COMPARATOR
UPPER ADDRESS COMPARATOR
LOWER ADDRESS COUNTERS
UPPER ADDRESS COUNTERS
CMDB0-7
CMDB8-15
LOADSP
LOADST
RUNEN
SEQSTR
RECYCLE
CMCPLSTR
CMCPL
SEG1672EN
SEG0EN
MCG
MCG2A
MCG2B
NREPEN
SPSTR
STSTR
LDCTSTR
CNTL MEM CNTREN
IOW
IOR
MRSTR
RECADSTR
MEMEOW
WAV REP CLK EN
WAVREPCLK
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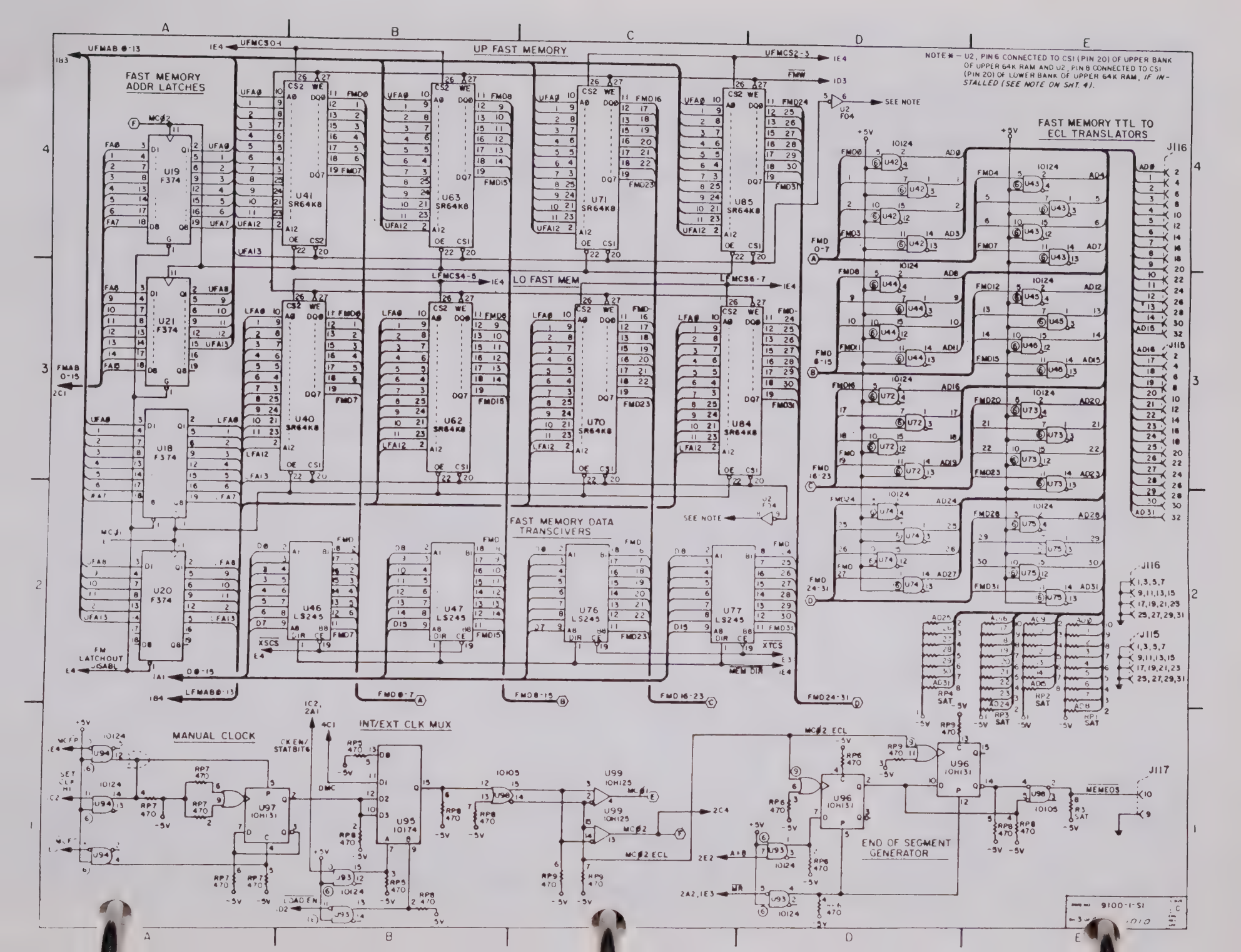
STATBIT5
CKEN/STATBIT8
STATBIT4
STATBIT2
STATBIT1
FMAB0-15
SPD0-15
FA0-15
J117


UP FAST MEMORY
FAST MEMORY ADDR LATCHES
LO FAST MEM
FAST MEMORY TTL TO ECL TRANSLATORS
FAST MEMORY DATA TRANSCIVERS
MANUAL CLOCK
INT/EXT CLK MUX
END OF SEGMENT GENERATOR
NOTE * – U2, PIN 6 CONNECTED TO CS1 (PIN 20) OF UPPER BANK OF UPPER 64K RAM AND U2, PIN 8 CONNECTED TO CS1 (PIN 20) OF LOWER BANK OF UPPER 64K RAM, IF INSTALLED (SEE NOTE ON SHT. 4).
SEE NOTE
U41 SR64K8
U63 SR64K8
U71 SR64K8
U85 SR64K8
U40 SR64K8
U62 SR64K8
U70 SR64K8
U84 SR64K8
U19 F374
U21 F374
U18 F374
U20 F374
U46 LS245
U47 LS245
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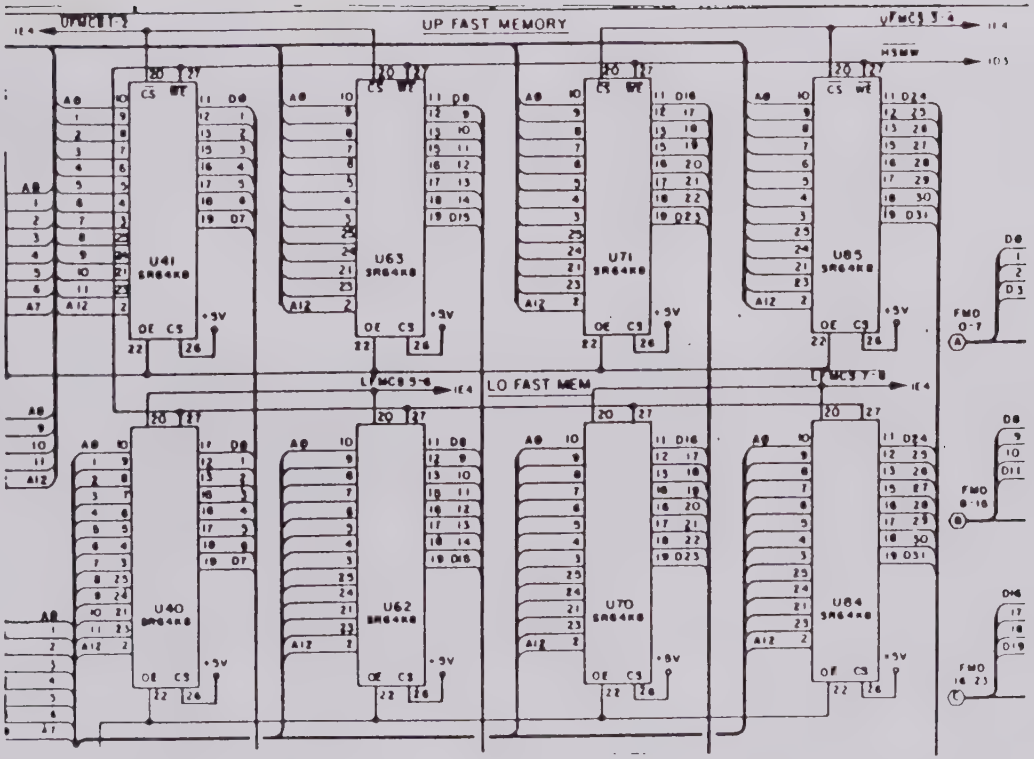
U97 10H131
U99 10H125
10124
10105
J116
J115
J117



NOTE: THIS PAGE OF SCHEMATIC REFLECTS CONNECTIONS FOR REV. E AND EARLIER 9100-1 BOARDS ONLY.

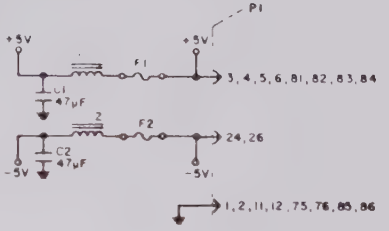
NOTE - AS AN OPTION, AN ADDITIONAL 64K RAM CAN BE INSTALLED AS FOLLOWS:

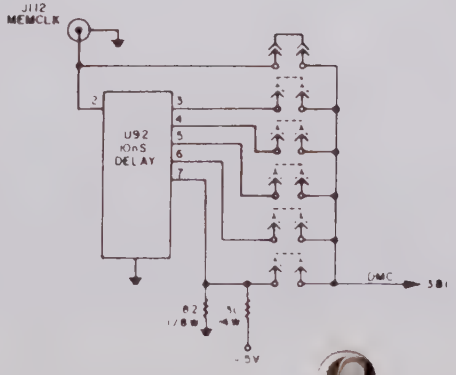
8 ADDITIONAL SR64K8's (205-270-064) PIGGY-BACKED ABOVE THE EXISTING ONES (U40, 41, 62, 63, 70, 71, 84 & 85). ALL PINS OF THE UPPER CHIPS MAY BE SOLDERED DIRECTLY TO THE CORRESPONDING PINS BELOW EXCEPT FOR PIN 20, WHICH MUST BE CONNECTED TO COMPLEMENTARY CHIP SELECT SIGNAL AVAILABLE AT A PAD ADJACENT TO PIN 20 OF THE EXISTING RAMS.

DEVICE	DESIGNATION	+5V	GND	-5V
CY7C128	U78, 79	24	12	
SR64K8	U40,41,62,63,70,71,84,85	28	14	
10H105	U98		1,16	8
10124	U42-45,U72-75, U93, 94	9	16	8
10H125	U99	9	16	8
10H131	U96, 97		1,16	8
10174	U95		1,16	8
74LS38	U3	14	7	
74F02	U37, 38	14	7	
74F04	U32, 2	14	7	
74F08	U6, 101	14	7	
74F10	U17	14	7	
74F11	U9, 28	14	7	
74F20	U16	14	7	
74F32	U10	14	7	
74F74	U4,7	14	7	
74F161	U22,25,U33-35,49,50,102-104	16	8	
74F164	U8	14	7	
74F244	U88,89	20	10	
74F374	U18-21	20	10	
74F377	U23,24,48,56,57,64,65	20	10	
74F521	U55,58	20	10	
74LS04	U52	14	7	
74LS08	U13, 36,	14	7	
74310	U39	14	7	
74LS11	U26	14	7	
74LS32	U5, 27,	14	7	
74LS74	U11,12,1	4	7	
74S138	U59	6	8	
74S139	U53	6	8	
74S240	U61,69,83	20	10	
74LS244	U14,66-68,80-82	20	10	
74LS245	U46,47,76,77,86,87	20	10	
74S260	U54	14	7	
74LS377	U90,105,106	20	10	
74LS541	U60	20	10	
74LS640	U91,107	20	10	
74S32	U30,31	14	7	
74LS00	U51	14	7	

SPARES

DESIG	PIN NO.
U2	1-4,10-13
U5	8-10
U6	4-6
U10	8-13
U13	1-3
U1	10-13
U100	ALL
U3	4-6, 8-13
U38	11-13
U53	9-15
U61	3,5,7,9,11,13,15,17,19
U94	1,3,7
U95	2-6
U98	6,7,9-11
U99	5-7, 10-12
U101	1-3, 8-13





LAST REFERENCE DESIGNATION USED

R2

LeCroy RESEARCH SYSTEMS

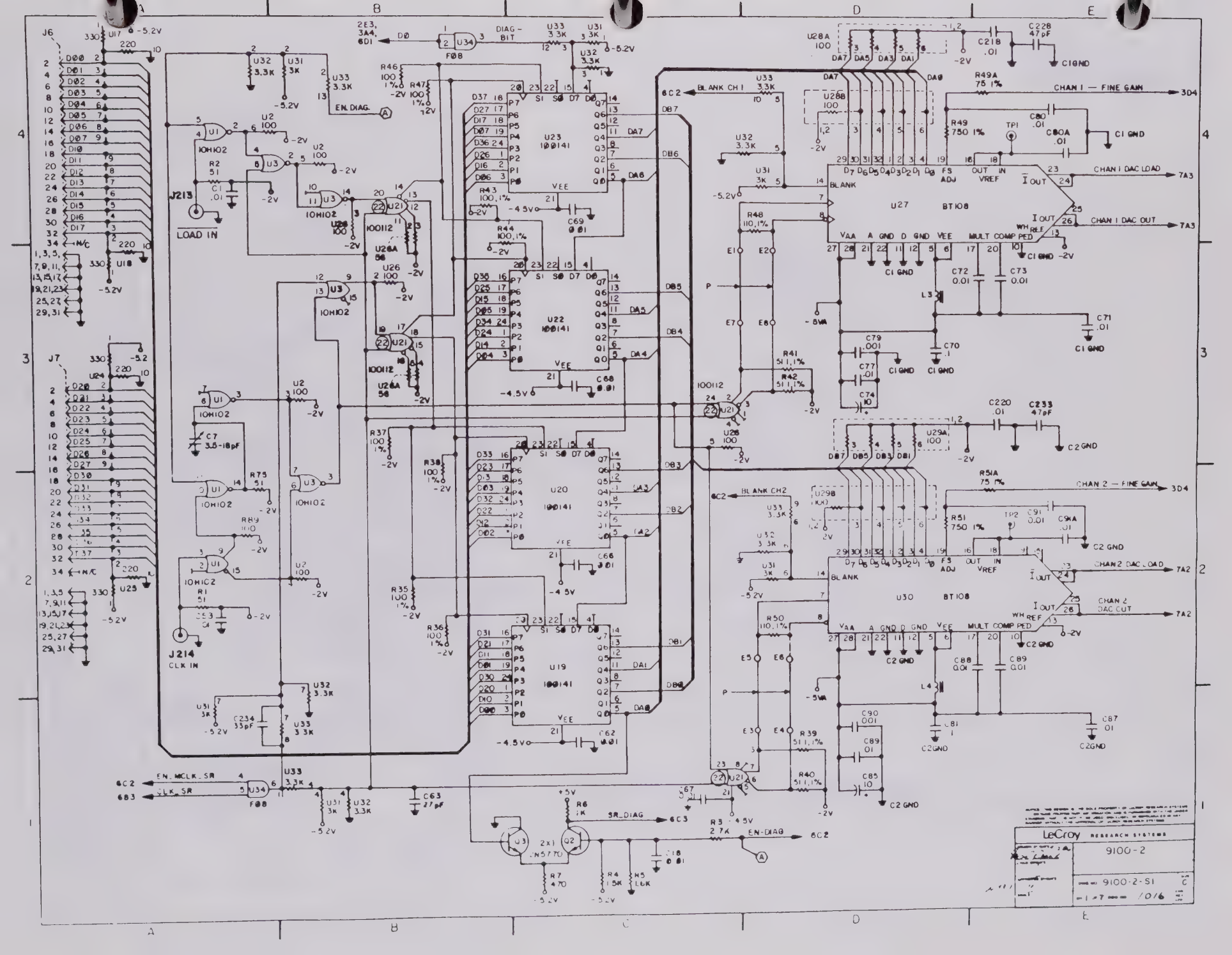
9100-1

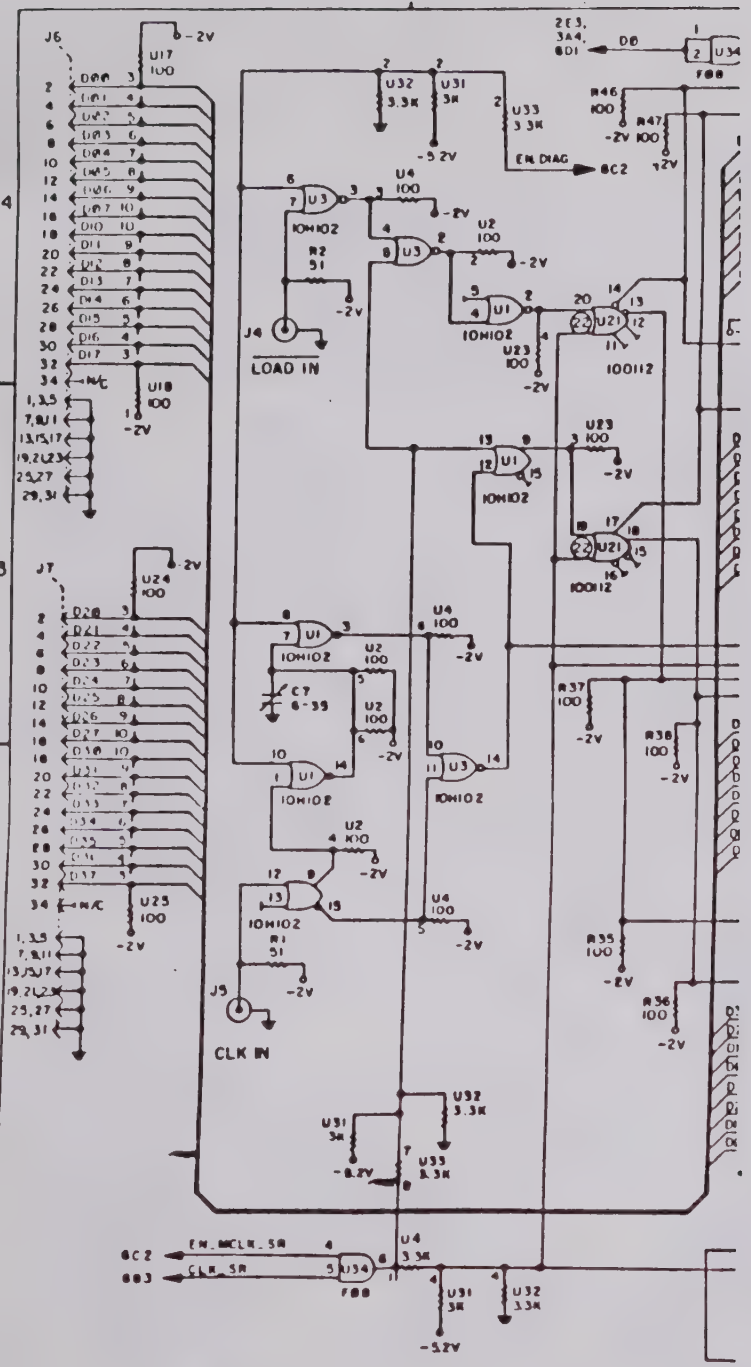
9100-1 Acronym Dictionary

Acronym	Definition
A=B	fast memory Address = stop address (B)
A0-19	multibus Address signals
AD0-31	Analog card Data inputs
CA0-10	Control Address signals
CCLK	multibus Clock C signal
CD0-15	Control memory address counter Data bus
CKEN/STATBIT6	Clock Enable / Status Bit 6
CMA0-10	Control Memory Address signals
CMAB0-10	Control Memory Address Bus
CMCPL	Control Memory Counter Parallel Load
CMCPLSTR	Control Memory Counter Parallel Load Strobe
CMCS	Control Memory Chip Select
CMD0-15	Control Memory Data signals
CMDB0-15	Control Memory Data Bus
CMW	Control Memory Write enable
CNTLMEMCNTREN	Control Memory Counter Enable
D0-15	multibus Data signals
DMC	Delayed Memory Clock
FA0-15	Fast memory Address signals
FMAB0-15	Fast Memory Address Bus
FMCS	Fast Memory Chip Select
FMD0-31	Fast Memory Data
FMLATCHOUTDISABL	Fast Memory address Latch Output Disable
FMW	Fast Memory Write enable
INIT	multibus Initialize signal
IOR	board I/O Read
IORC	multibus I/O Read Command signal
IOSEL	board I/O Select
IOSTR	board I/O Strobe (Port Address 580)
IOW	board I/O Write
IOWC	multibus I/O Write Command signal
LDCTSTR	segment repetition Counter (& Control word) parallel Load Strobe
LFA0-13	Lower Fast memory Address signals
LFMAB0-13	Lower Fast Memory Address Bus
LFMCS4-7	Lower Fast Memory Chip Select 4-7
LOADEN	Load Enable
LOADSP	Load StoP address holding register
LOADST	Load StarT address holding register
MCϕ1	Memory Clock Phase 1
MCϕ2	Memory Clock Phase 2 (TTL Level)
MCϕ2A,B	gated Memory Clocks, Phase 2 (A & B)
MCϕ2ECL	Memory Clock Phase 2 (ECL Level)
MCFC	Manual Clock Flop Clear
MCFP	Manual Clock Flop Preset

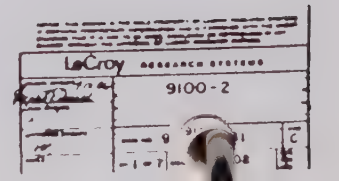
9100-1 Acronym Dictionary

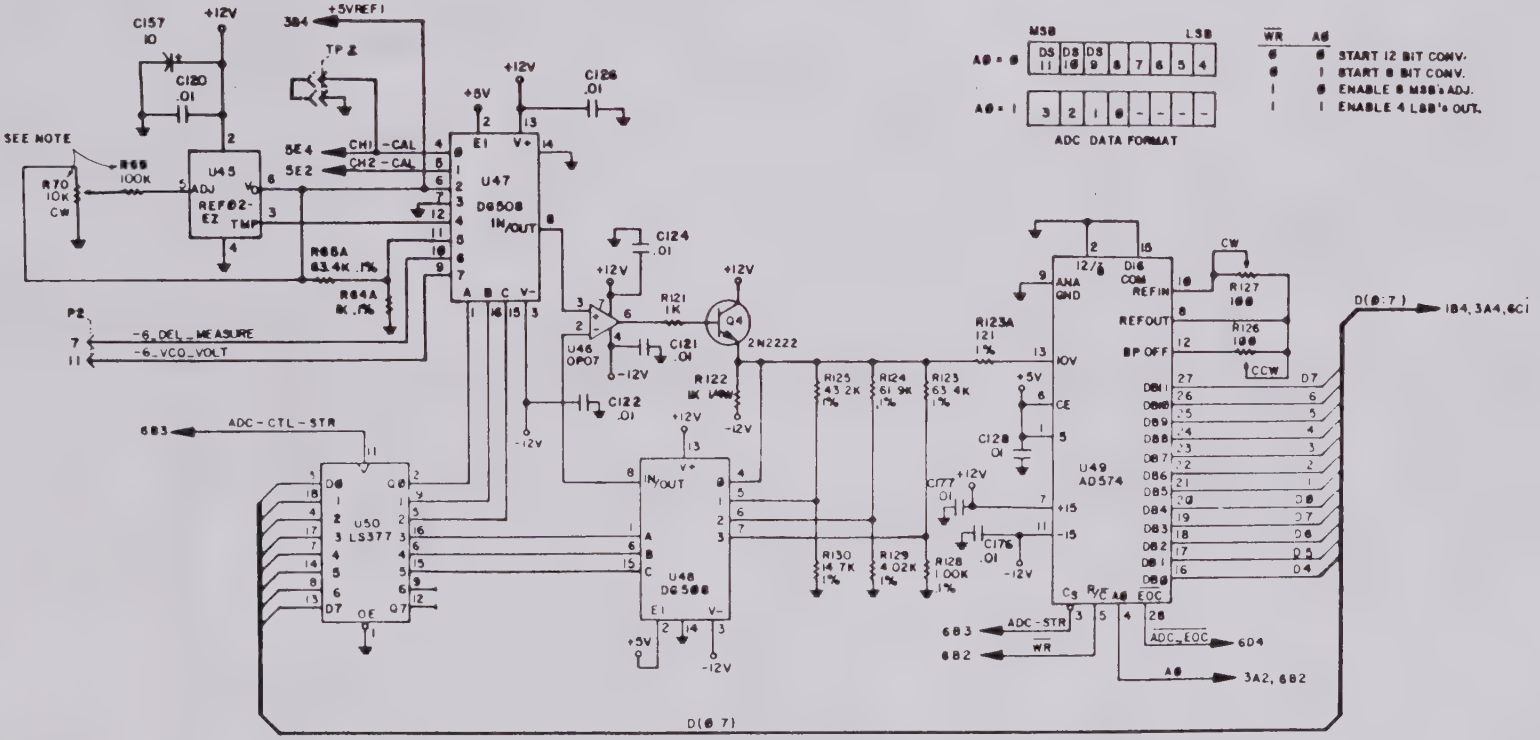
Acronym	Definition
MEMCLK	Memory Clock (from -6)
MEMDIR	Memory Direction control
MEMEOS	Memory End Of Segment
MEMEOW	Memory End Of Waveform
MR	Master Reset
MRDC	multibus Memory Read Command signal
MRSTR	Master Reset Strobe
MWTC	multibus Memory Write Command signal
NREPEN	segmeNt Repetition counter Enable
RECADSTR	Recycle Address Strobe
RECYCLE	Recycle
RUNEN	Run Enable
SEG1672EN	Segment length ≥16-bit, <72-bit Enable
SEG8EN	8-bit Segment Enable
SETCLKHI	Set manual Clock High
SPD0-7	Stop Data Bus (lower bits)
SPD8-15	Stop Data Bus (upper bits)
SPSTR	StoP address holding register parallel load Strobe
ST/SPPLSTR	StarT & StoP address counter Parallel Load Strobe
STATBIT1-5	Status Bits
STSTR	StarT address holding register parallel load Strobe
UFA0-13	Upper Fast memory Address signals
UFMAB0-13	Upper Fast Memory Address Bus
UFMCS0-3	Upper Fast Memory Chip Select 0-3
WAVREPCLK	Waveform Repetition Clock
WAVREPCLKEN	Waveform Repetition Clock Enable
XACK	multibus Acknowledge signal
XSCS	eXternal data tranSceiver Chip Select (low 16 bits)
XTCS	eXternal data Transceiver Chip Select (hi 16 bits)


J6
J7
J213
LOAD IN
J214
CLK IN
U23 100141
U22 100141
U20 100141
U19 100141
U27 BT108
U30 BT108
CHAN 1 — FINE GAIN
CHAN 2 — FINE GAIN
CHAN 1 DAC LOAD
CHAN 1 DAC OUT
CHAN 2 DAC LOAD
CHAN 2 DAC OUT
BLANK CH 1
BLANK CH2
EN. DIAG.
EN-DIAG
SR_DIAG
EN. MCLK_SR
CLK_SR
LeCroy RESEARCH SYSTEMS
9100-2
9100-2-SI



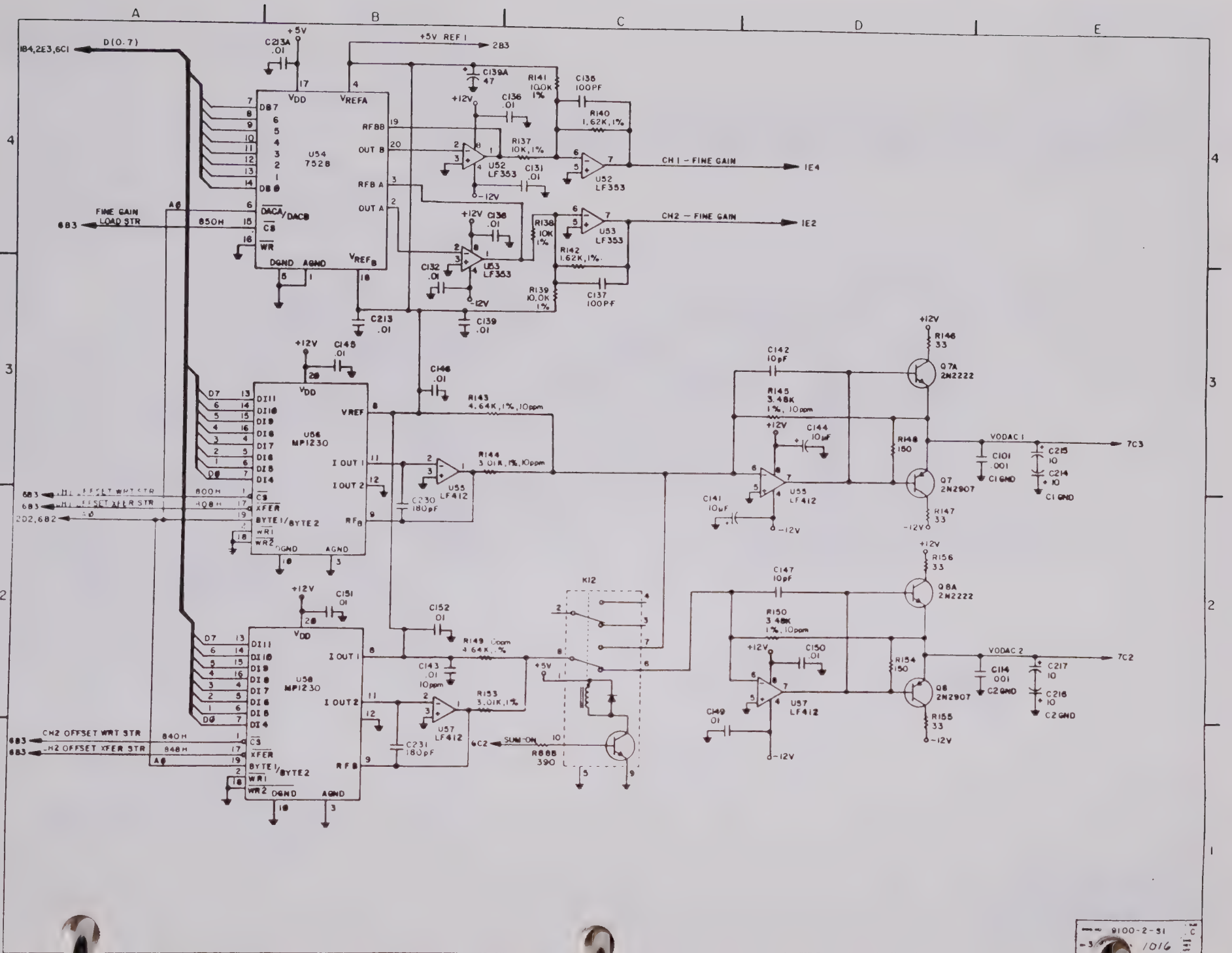
NOTE: THIS PAGE OF SCHEMATIC REFLECTS CONNECTIONS FOR REV. C AND REV. D 9100-2 BOARDS ONLY.

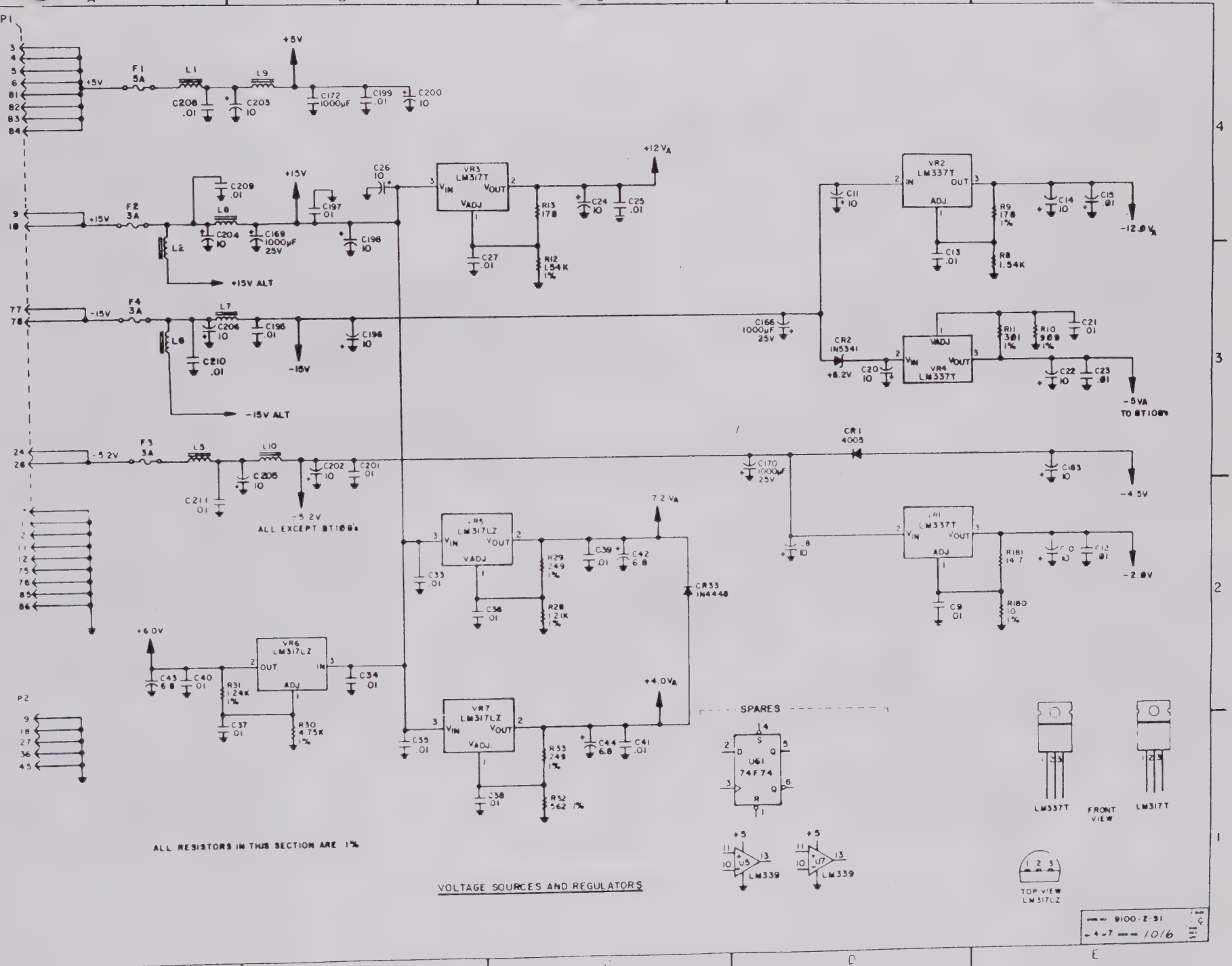


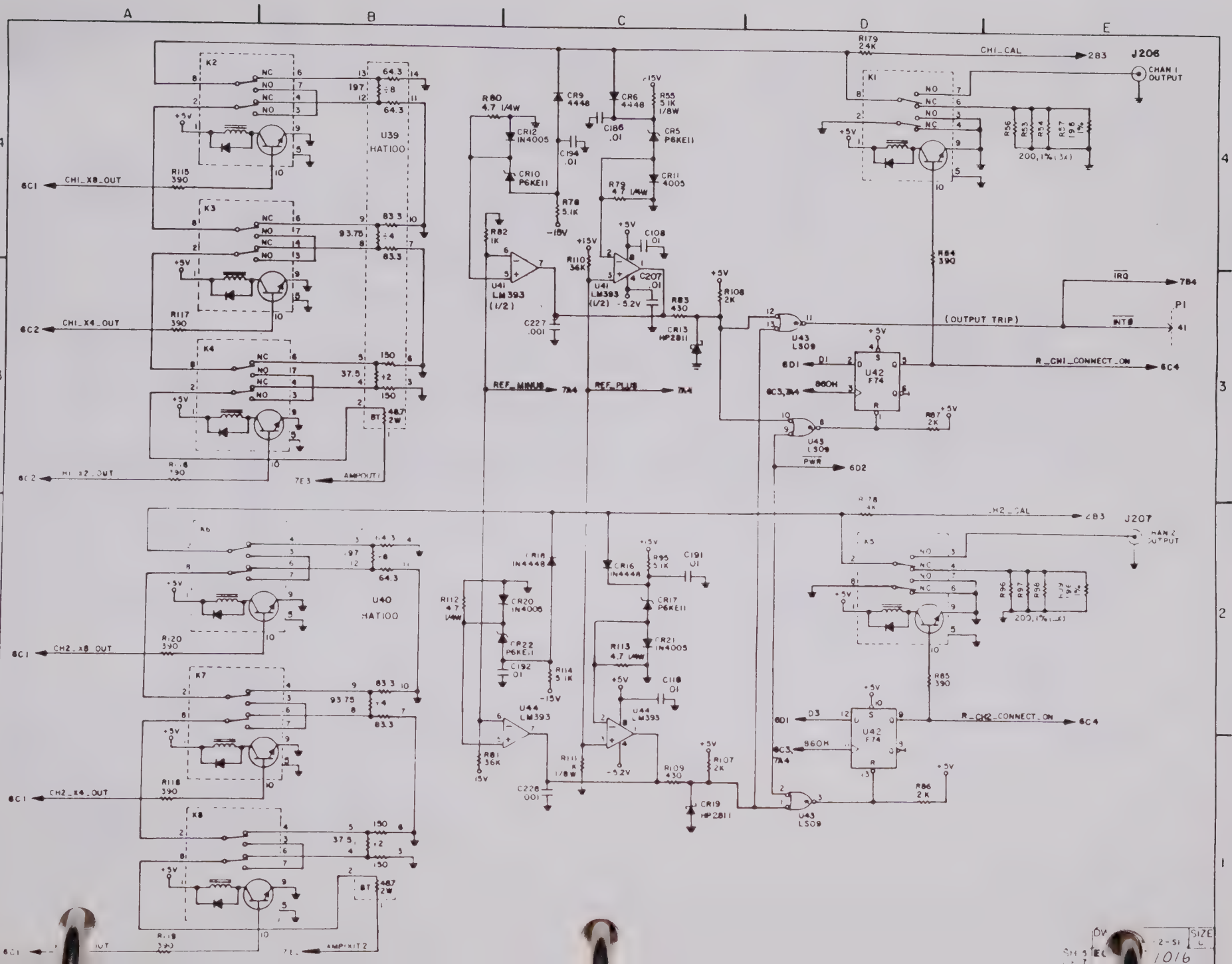


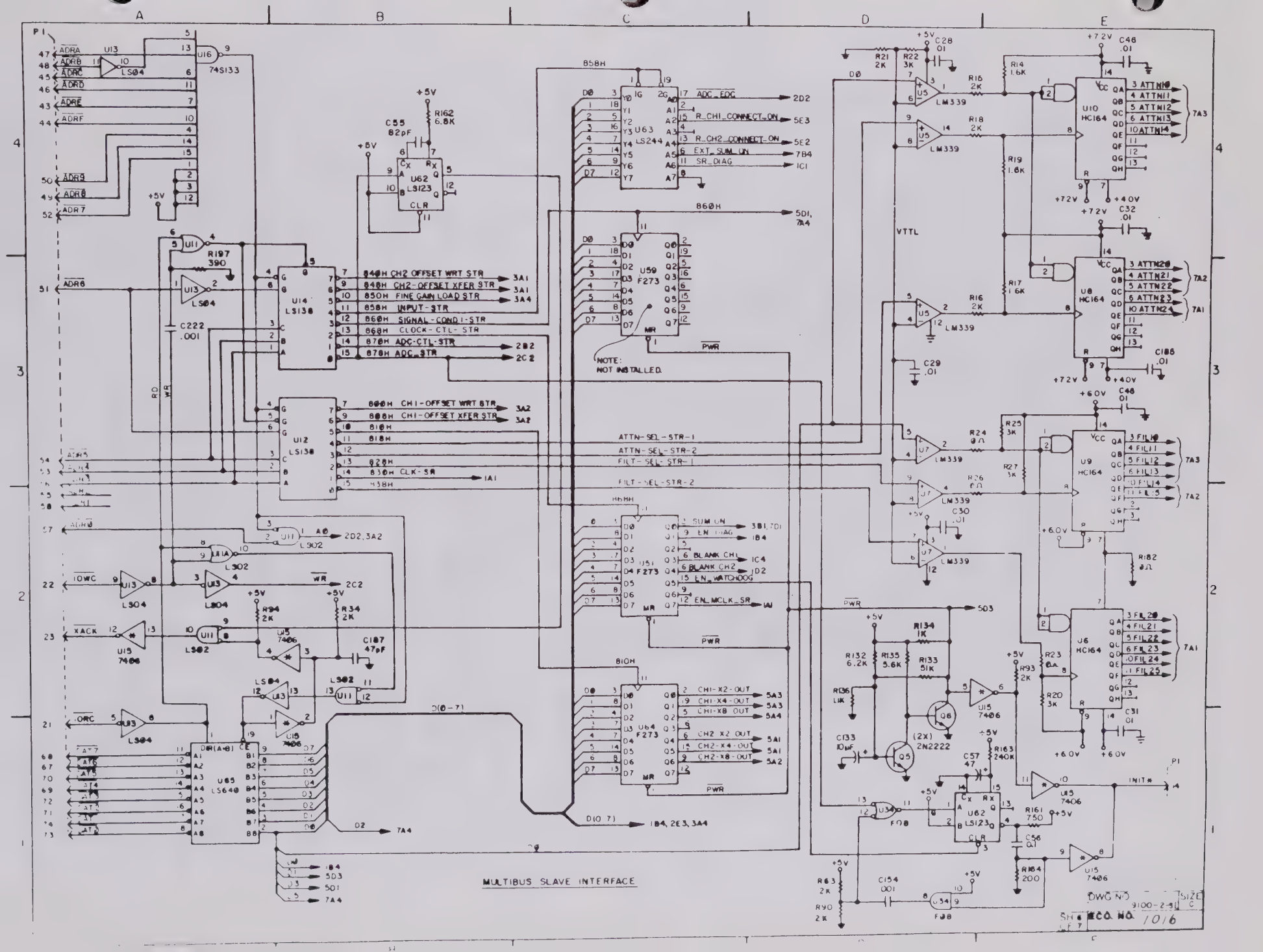
NOTE
R69 AND R70 NOT INSTALLED

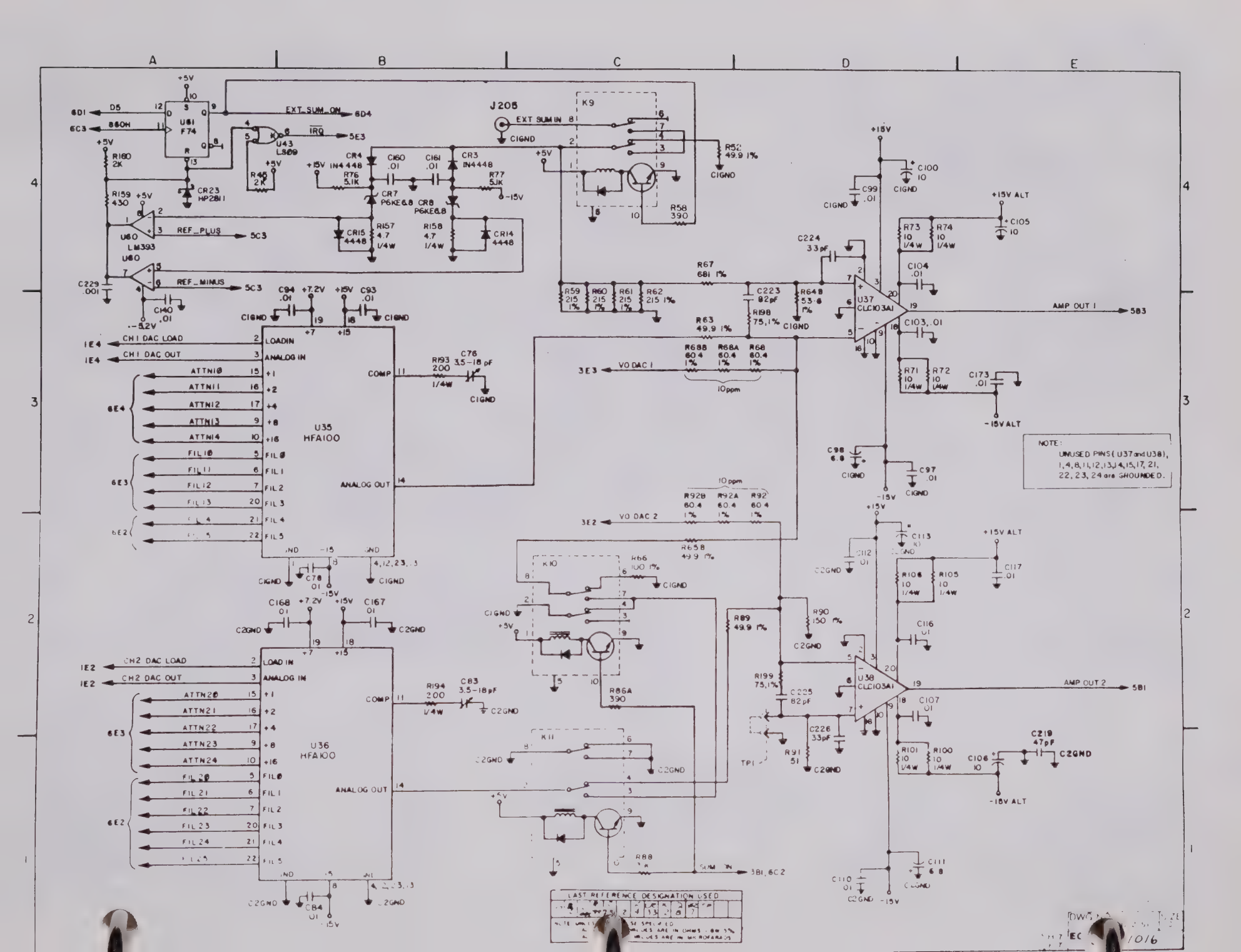
DWG NO. 400-2-51 SIZE C
ECO. NO. 1016


D(0.7)
+5V
+5V REF I
CH1 – FINE GAIN
CH2 – FINE GAIN
FINE GAIN LOAD STR
U54 7528
U52 LF353
U53 LF353
U56 MP1230
U58 MP1230
U55 LF412
U57 LF412
Q7A 2N2222
Q7 2N2907
Q8A 2N2222
Q8 2N2907
VODAC 1
VODAC 2
CH2 OFFSET WRT STR
CH2 OFFSET XFER STR
SUM ON
VDD
VREFA
VREFB
DGND
AGND
VREF
I OUT 1
I OUT 2
BYTE1/BYTE2


P1
+5V
F1 5A
L1
L9
C208 .01
C203 10
C172 1000µF
C199 .01
C200 10
+15V
F2 3A
L8
L2
C209 .01
C204 10
C169 1000µF 25V
C197 .01
C198 10
C26 10
VR3 LM317T
VADJ
R13 178
R12 1.54K 1%
C27 .01
C24 10
C25 .01
+12VA
+15V ALT
-15V
F4 3A
L7
L6
C206 10
C196 .01
C210 .01
C195 10
-15V ALT
-5.2V
F3 3A
L5
L10
C205 10
C202 10
C201 .01
C211 .01
-5.2V ALL EXCEPT BT108
VR2 LM337T
ADJ.
R9 178 1%
R8 1.54K
C11 10
C13 .01
C14 10
C15 .01
-12.8VA
C166 1000µF 25V
CR2 IN5341
+6.2V
C20 10
VR4 LM337T
R11 301 1%
R10 909 1%
C21 .01
C22 10
C23 .01
-5VA TO BT108
CR1 4005
C170 1000µF 25V
C183 10
-4.5V
VR1 LM337T
R18I 147
R180 10 1%
C9 .01
C10 10
C12 .01
-2.8V
VR5 LM317LZ
R29 249 1%
R28 12.1K 1%
C33 .01
C36 .01
C39 .01
C42 6.8
7.2VA
CR33 IN4448
VR6 LM317LZ
+6.0V
R31 124K 1%
R30 4.75K 1%
C43 6.8
C40 .01
C37 .01
C34 .01
VR7 LM317LZ
R33 249 1%
R32 562 1%
C35 .01
C38 .01
C44 6.8
C41 .01
+4.0VA
P2
SPARES
U61 74F74
U5 LM339
U7 LM339
+5
LM337T
FRONT VIEW
LM317T
TOP VIEW LM317LZ
ALL RESISTORS IN THIS SECTION ARE 1%
VOLTAGE SOURCES AND REGULATORS
9100-2-31
4 of 7
10/6


A
B
C
D
E
K2
K3
K4
K1
U39
HAT100
CH1_X8_OUT
CH1_X4_OUT
CH1_X2_OUT
AMPEXIT1
CH1_CAL
J206
CHAN 1 OUTPUT
R80 4.7 1/4W
CR12 IN4005
CR10 P6KE11
R78 5.1K
-15V
CR9 4448
CR6 4448
C186 .01
C194 .01
R55 5.1K 1/8W
CR5 P6KE11
CR11 4005
R79 4.7 1/4W
R82 1K
U41 LM393 (1/2)
R110 36K
C207 .01
U41 LM393 (1/2) -5.2V
C108 .01
C227 .001
R83 430
CR13 HP2811
R108 2K
R84 390
R56 R53 R54 R57 200,1%(3X)
IRQ
INT8
P1
(OUTPUT TRIP)
U43 LS09
U42 F74
D1
860H
R_CH1_CONNECT_ON
PWR
REF_MINUS
REF_PLUS
K6
K7
K8
U40
HAT100
CH2_X8_OUT
CH2_X4_OUT
CH2_X2_OUT
AMPEXIT2
CH2_CAL
J207
CHAN 2 OUTPUT
CR18 IN4448
CR20 IN4006
CR22 P6KE11
C192 .01
R114 5.1K
CR16 IN4448
R99 5.1K
C191 .01
CR17 P6KE11
CR21 IN4005
R113 4.7 1/4W
C118 .01
U44 LM393
R112 4.7 1/4W
R81 36K
R111 1/8W
-5.2V
C228 .001
R109 430
R107 2K
CR19 HP2811
R85 390
R96 R97 R98 200,1%(3X)
D3
R_CH2_CONNECT_ON
R86 2K
U43 LS09
SIZE C
1016


MULTIBUS SLAVE INTERFACE
NOTE: NOT INSTALLED
DWG NO 9100-2-01
SIZE C
ECO NO 1016
SHT 6 OF 7


A
B
C
D
E
U61 F74
U43 LS09
U60 LM393
U35 HFA100
U36 HFA100
U37 CLC103AI
U38 CLC103AI
J205
K9
K10
K11
EXT SUM IN
EXT SUM ON
REF_PLUS
REF_MINUS
CH1 DAC LOAD
CH1 DAC OUT
CH2 DAC LOAD
CH2 DAC OUT
VO DAC 1
VO DAC 2
AMP OUT 1
AMP OUT 2
SUM IN
+15V ALT
-15V ALT
CIGND
C2GND
NOTE:
UNUSED PINS (U37 and U38), 1, 4, 8, 11, 12, 13, 14, 15, 17, 21, 22, 23, 24 are GROUNDED.

9100-2 Acronym Dictionary

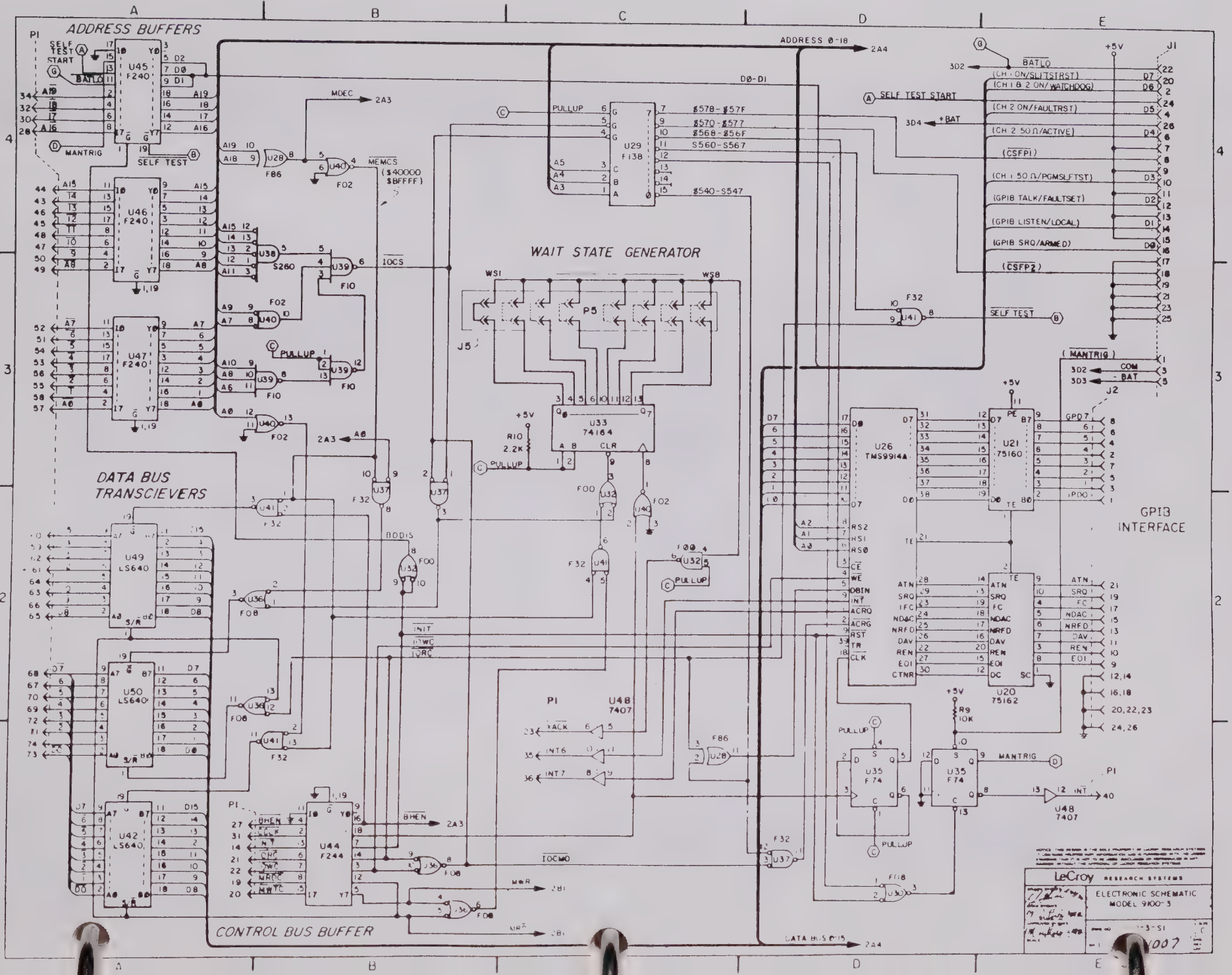
Acronym	Definition
+5VREF1	+5V Reference, Accurate to +/- 15mV
-6_DEL_MEASURE	-6 trig Delay Measurement; 0V = 0nS, then +10mV/nS
-6_VCO_VOLT	-6 Voltage Controlled Oscillator control Voltage/2
A0	Address 0
ADC-CTL-STR	ADC Control Strobe
ADC-STR	ADC Strobe
ADC_EOC/	ADC End of Conversion
ADR0/ to ADRA/	16 bit Multibus Address Bus
AMP OUT 1	Direct Output of Channel 1 Amplifier
AMP OUT 2	Direct Output of Channel 2 Amplifier
ATTEN-SEL-STR-1	Attenuator Select Strobe for Channel 1
ATTEN-SEL-STR-2	Attenuator Select Strobe for Channel 2
ATTEN10	Channel 1 Pre Amp x 1 Atten on
ATTEN11	Channel 1 Pre Amp x 2 Atten on
ATTEN12	Channel 1 Pre Amp x 4 Atten on
ATTEN13	Channel 1 Pre Amp x 8 Atten on
ATTEN14	Channel 1 Pre Amp x 16 Atten on
ATTEN20	Channel 2 Pre Amp x 1 Atten on
ATTEN21	Channel 2 Pre Amp x 2 Atten on
ATTEN22	Channel 2 Pre Amp x 4 Atten on
ATTEN23	Channel 2 Pre Amp x 8 Atten on
ATTEN24	Channel 2 Pre Amp x 16 Atten on
BLANK_CH_1	Blank Channel 1 (disables digital input codes)
BLANK_CH_2	Blank Channel 2 (disables digital input codes)
C1GND	Channel 1 Ground Plane
C2GND	Channel 2 Ground Plane
CH 2 CAL	Channel 2 Calibration input to ADC mux
CH 1-CAL	Channel 1 Calibration input to ADC mux
CH1 OFFSET XFER STR	Channel 1 Offset Dac Transfer Strobe (I/O port 808h)
CH1 OFFSET WRT STR	Channel 1 Offset Dac Write Strobe (I/O port 800h)
CH1_X2_OUT	Channel 1 Post Amp x 2 Atten on
CH1_X4_OUT	Channel 1 Post Amp x 4 Atten on
CH1_X8_OUT	Channel 1 Post Amp x 8 Atten on
CH2 OFFSET XFER STR	Channel 2 Offset Dac Transfer Strobe (I/O port 848h)
CH2 OFFSET WRT STR	Channel 2 Offset Dac Write Strobe (I/O port 840h)
CH2_X2_OUT	Channel 2 Post Amp x 2 Atten on
CH2_X4_OUT	Channel 2 Post Amp x 4 Atten on
CH2_X8_OUT	Channel 2 Post Amp x 8 Atten on
CHAN 2 DAC OUT	Same as for channel 1, except for channel 2

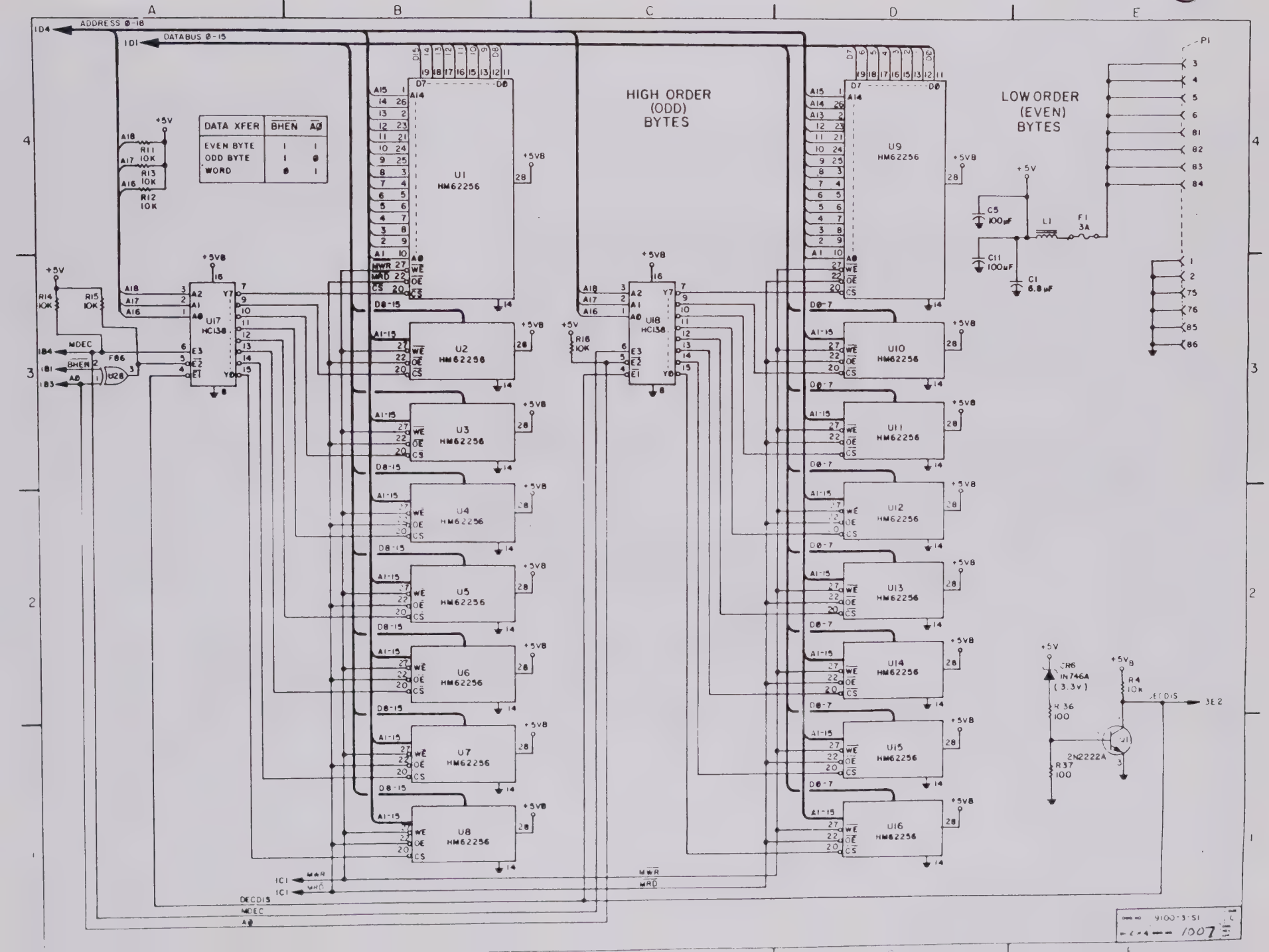
9100-2 Acronym Dictionary

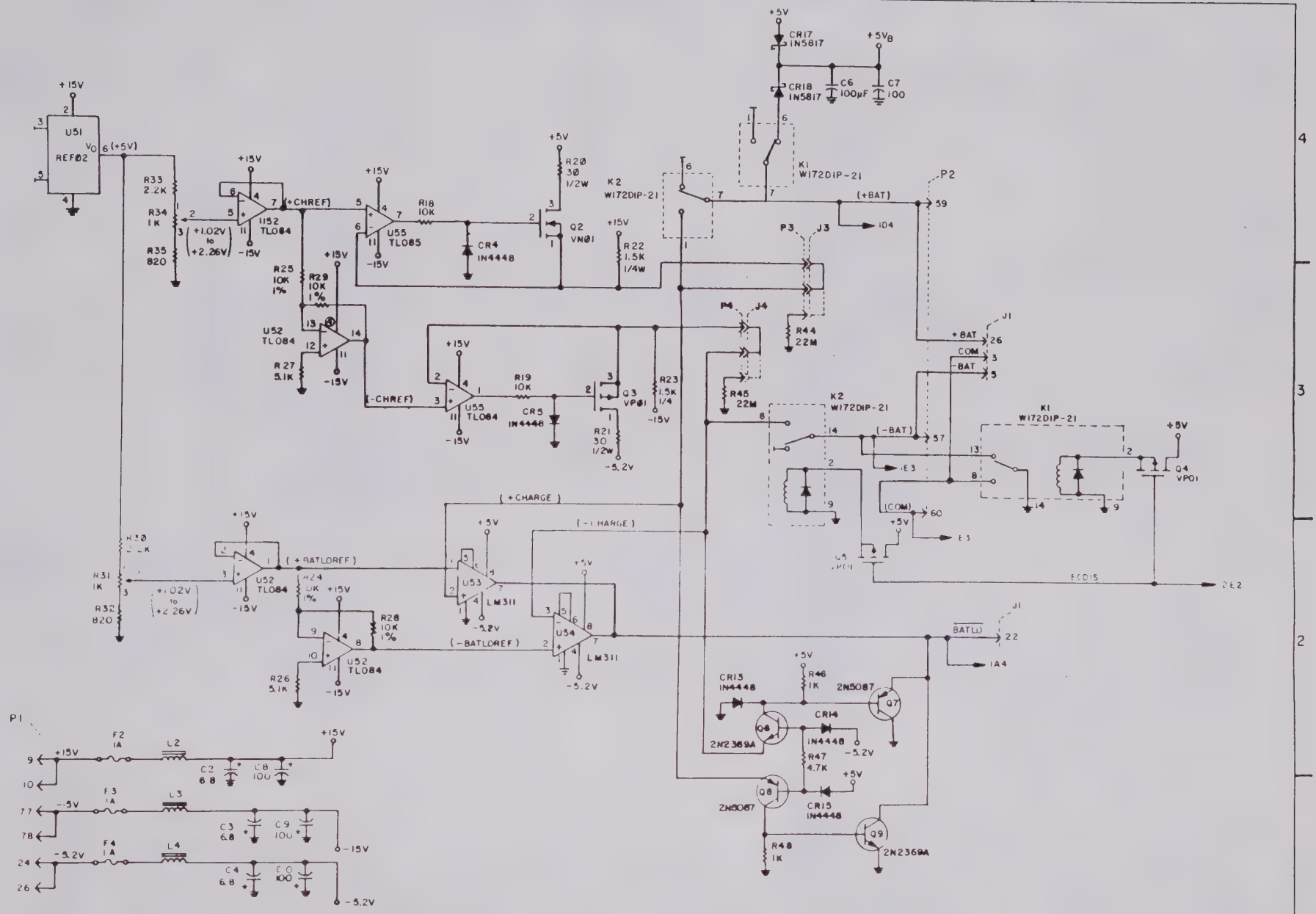
Acronym	Definition
CHAN 1 DAC OUT	Channel 1 Dac Output, Output of Signal Dac going to HFA100, 255 ~ 0V, 0 causes Signal Dac to go negative.
CHAN 2 DAC LOAD	Same as for channel 1, except for channel 2
CHAN 1 DAC LOAD	Channel 1 Dac Load, Output of Signal Dac; 0 ~ 0V, 255 causes Signal Dac to be Negative going
CHAN 2-FINE GAIN	Same as for channel 1, except for channel 2
CHAN 1-FINE GAIN	Channel 1 Fine Gain, analog level 0VDC ~ max gain, -.7V ~ min gain of Signal Dac
CLK IN/	Clock in From 9100-6 (ECL); aka "analog clock"
CLK_SR	Clock to Shift Register
CLOCK-CTL-STR	Write Strobe for port 868h
D(0:7)	Internal Bi-directional 8 bit data bus
D##	32 Bit Data Bus in ECL from 9100-1; First # is byte # followed by bit # within byte.
DA0-7	8 Bit Data Bus to Channel 1 Signal Dac (ECL)
DAT0/ to DAT7/	8 bit Multibus Bidirectional Data Bus
DB0-7	8 Bit Data Bus to Channel 2 Signal Dac (ECL)
DIAG_BIT	Diagnostic Bit, Serial input to 100141 SR
EN. DIAG.	Enable Diagnositics
EN_MCLK_SR	Enable Manual Clock to Shift Register (100141s)
EN_WATCHDOG	Enable Watchdog Timer
EXT SUM IN	External Sum Input
EXT_SUM_ON	External Sum mode turned On
FIL-SEL-STR-1	Filter Select Strobe for Channel 1
FIL-SEL-STR-2	Filter Select Strobe for Channel 2
FIL10	Channel 1 Fil 0 on (no filter)
FIL11	Channel 1 Fil 1 on (100 MHz filter)
FIL12	Channel 1 Fil 2 on (30 MHz filter)
FIL13	Channel 1 Fil 3 on (10 MHz filter)
FIL14	Channel 1 Fil 4 on (3 MHz filter)
FIL15	Channel 1 Fil 5 on (1 MHz filter)
FIL20	Channel 2 Fil 0 on (no filter)
FIL21	Channel 2 Fil 1 on (100 MHz filter)
FIL22	Channel 2 Fil 2 on (30 MHz filter)
FIL23	Channel 2 Fil 3 on (10 MHz filter)
FIL24	Channel 2 Fil 4 on (3 MHz filter)
FIL25	Channel 2 Fil 5 on (1 MHz filter)
FINE GAIN LOAD STR	Fine Gain Dac Load Strobe (I/O port 850h)

9100-2 Acronym Dictionary

Acronym	Definition
INIT*	Multibus Init Line
INPUT-STR	Input Strobe, active low for read to Multibus
INT0/	Interrupt 0, aka IRQ/
IORC/	Input, Output Read Command
IOWC/	Input, Output Write Command
IRQ/	Interrupt Request, aka INT0/
LOAD IN/	Load in From 9100-6 (ECL)
PWR/	Power Up Reset, active low
R_CH1_CONNECT_ON	Relay drive to channel 1 connect relay
R_CH2_CONNECT_ON	Relay drive to channel 2 connect relay
RD	Read
REF_MINUS	Reference Minus (~-400mV)
REF_PLUS	Reference Plus (~+400mV)
SIGNAL-CONDI-STR	Write Strobe for port 860h
SR_DIAG	Shift Register Diagnostics
SUM-ON	Internal Channel Sum On
VODAC 2	Output of Offset Dac for Channel 2
VODAC 1	Output of Offset Dac for Channel 1
WR/ or WR	Write
XACK/	Transfer Acknowledge


ADDRESS BUFFERS
DATA BUS TRANSCIEVERS
WAIT STATE GENERATOR
GPIB INTERFACE
CONTROL BUS BUFFER
ADDRESS 0-18
D0-D1
U45 F240
U46 F240
U47 F240
U49 LS640
U50 LS640
U42 LS640
U44 F244
U29 F138
U33 74164
U26 TMS9914A
U21 75160
U20 75162
U35 F74
U48 7407
SELF TEST START
MANTRIG
SELF TEST
MDEC
MEMCS (S40000 SBFFFF)
IOCS
IOCWO
BHEN
INIT
IOWC
IORC
MWR
MRR
DATA BUS 0-15
LeCroy RESEARCH SYSTEMS
ELECTRONIC SCHEMATIC
MODEL 9100-3


ADDRESS 0-18
DATABUS 0-15
DATA XFER | BHEN | A0
EVEN BYTE | 1 | 1
ODD BYTE | 1 | 0
WORD | 0 | 1
HIGH ORDER (ODD) BYTES
LOW ORDER (EVEN) BYTES
U1 HM62256
U2 HM62256
U3 HM62256
U4 HM62256
U5 HM62256
U6 HM62256
U7 HM62256
U8 HM62256
U9 HM62256
U10 HM62256
U11 HM62256
U12 HM62256
U13 HM62256
U14 HM62256
U15 HM62256
U16 HM62256
U17 HC138
U18 HC138
MDEC
BHEN
A0
DECDIS
MWR
MRD
+5V
+5VB
P1
C5 100µF
C11 100µF
C1 6.8µF
L1
F1 3A
CR6 IN746A (3.3V)
R36 100
R37 100
R4 10K
2N2222A
Q1
3E2


U51 REF02
+15V
+5V
-15V
-5.2V
R33 2.2K
R34 1K
R35 820
+1.02V to +2.26V
U52 TL084
U55 TL085
+CHREF
-CHREF
R18 10K
R19 10K
R20 30 1/2W
R21 30 1/2W
R22 1.5K 1/4W
R23 1.5K 1/4
R25 10K 1%
R26 5.1K
R27 5.1K
R28 10K 1%
R29 10K 1%
R30 2.2K
R31 1K
R32 820
R44 22M
R45 22M
Q2 VN01
Q3 VP01
Q4 VP01
CR4 IN4448
CR5 IN4448
CR13 IN4448
CR14 IN4448
CR15 IN4448
CR17 IN5817
CR18 IN5817
C6 100pF
C7 100
C2 6.8
C3 6.8
C4 6.8
C8 100
C9 100
C0 100
F2 1A
F3 1A
F4 1A
L2
L3
L4
K1 W172DIP-21
K2 W172DIP-21
P1
P2
P3 J3
P4 J4
J1
+BAT
-BAT
COM
+BATLOREF
-BATLOREF
+CHARGE
-CHARGE
LM311
2N2369A
2N5087
2N6067
Q7
Q8
Q9
R46 1K
R47 4.7K
R48 1K
ECDIS
BATLO

VOLTAGE AND GROUND PIN CHART

DEVICE	REFERENCE DESIGNATION	+5V	+5VB	GND	+15V	-15V	-52V
74F240	U45-47	20		10			
74LS640	U42,49,50	20		10			
74F244	U44	20		10			
74F138	U29	16		8			
74164	U33	14		7			
74F74	U35	14		7			
TMS9914A	U26	40		20			
75160	U21	20		10			
75162	U20	22		11			
74HC138	U17,18		16	8			
HM62256	U1-U16		28	14			
REF02	U51			4	2		
74F260	U38	14		7			
74F10	U39	14		7			
74F02	U40	14		7			
74F86	U28	14		7			
74F32	U41,37	14		7			
74F08	U30,36	14		7			
74F00	U32	14		7			
74C7	U48	4		7			
TL084	U52,55				4		
LM311	U53,54	8					8

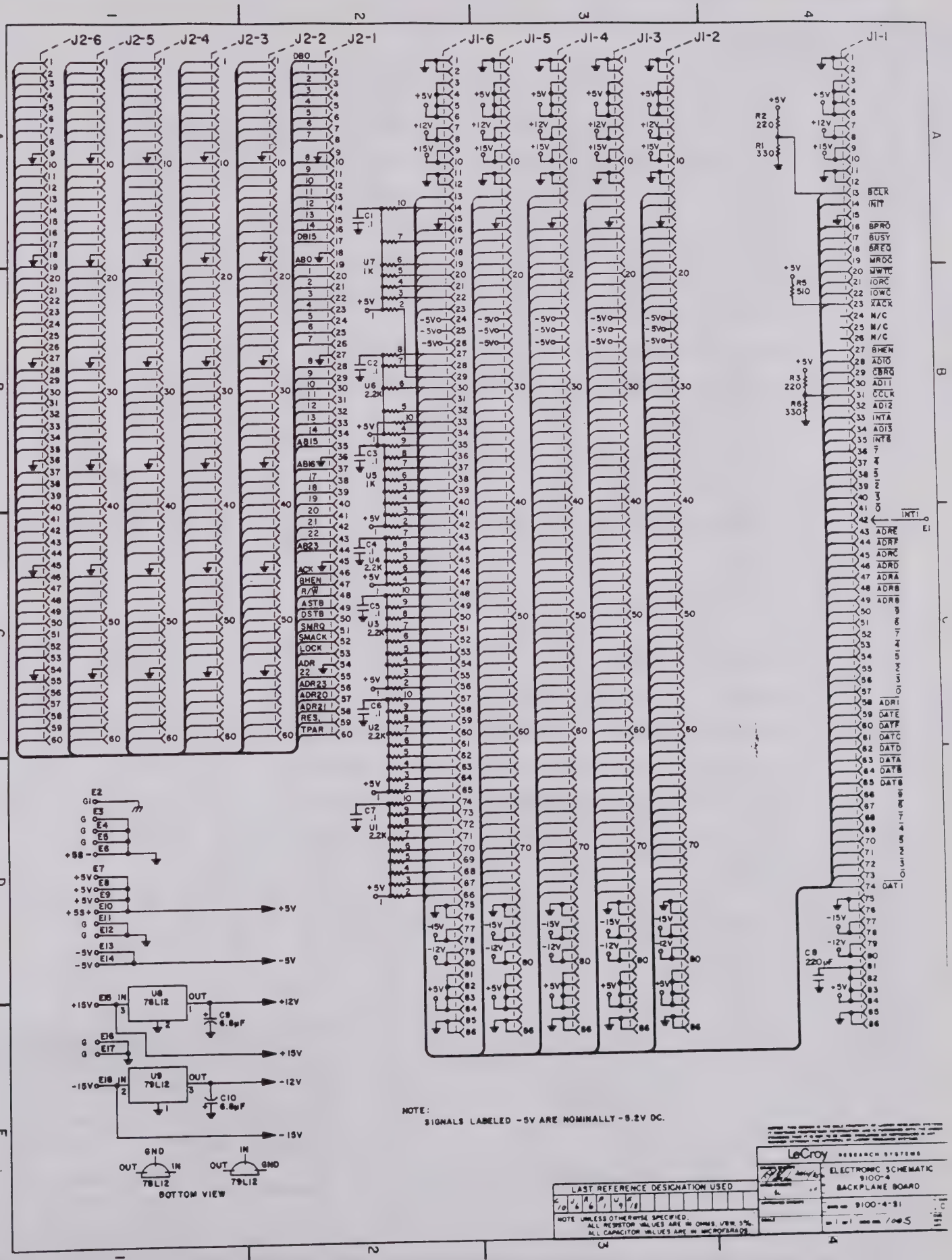
SPARE PINS

DEVICE	REFERENCE DESIGNATION	PIN NO.
74S260	U38	4,6,8,9,10,11
74F86	U28	4,5,6
74F08	U30	4,5,6,8,9,10,11,12,13
74F00	U32	11,12,13
74C7	U48	1,2,3,4
74F32	U37	4,5,6
TL084	U55	8,9,10,12,13,14

LAST REFERENCE DESIGNATION USED

9100-3 Acronym Dictionary

Acronym	Definition
+5VB	positive 5V supply backup
+BAT	positive battery line
+BATLOREF	positive battery low reference
+CHARGE	positive battery voltage
+CHREF	positive battery charge reference
-BAT	negative battery line
-BATLOREF	negative battery low reference
-CHARGE	negative battery voltage
-CHREF	negative battery charge reference
A19-A0	address lines (MultiBus)
ACTIVE	channel active LED
ARMED	armed LED
ATN	attention (GPIB)
BATLO	battery low
BDDIS	board disable
BHEN	data bus high enable (MultiBus)
CCLK	common clock (MultiBus)
COM	common battery line
CSFP1	chip select front panel #1
CSFP2	chip select front panel #2
D15-D0	data lines (MultiBus)
DAV	data valid (GPIB)
DECDIS	decoder disable
EOI	end or identify (GPIB)
FAULTRST	fault LED reset
FAULTSET	fault LED set
GPD7-GPD0	data lines (GPIB)
IFC	interface clear (GPIB)
INIT	power-up initialization (MultiBus)
INT6	interrupt 6-GPIB transfer interrupt (MultiBus)
INT7	interrupt 7-GPIB DMA interrupt (MultiBus)
IORC	I/O read cycle (MultiBus)
IOWC	I/O write cycle (MultiBus)
LOCAL	GPIB local LED
MANTRIG	manual trigger pushbutton
MEMCS	memory chip select
MRDC	memory read cycle (Multibus)
MWTC	memory write cycle (MultiBus)
NDAC	no data accepted (GPIB)
NRFD	not ready for data (GPIB)
PGMSLFTST	program self test LED
REN	remote enable (GPIB)
SELFTEST	self test start decode
SELFTESTSTART	self test start pushbutton
SLFTSTRST	self test LED reset
SRQ	service request (GPIB)
WATCHDOG	watchdog timer
XACK	board cycle acknowledge (MultiBus)



NOTE:
SIGNALS LABELED -5V ARE NOMINALLY -5.2V DC.

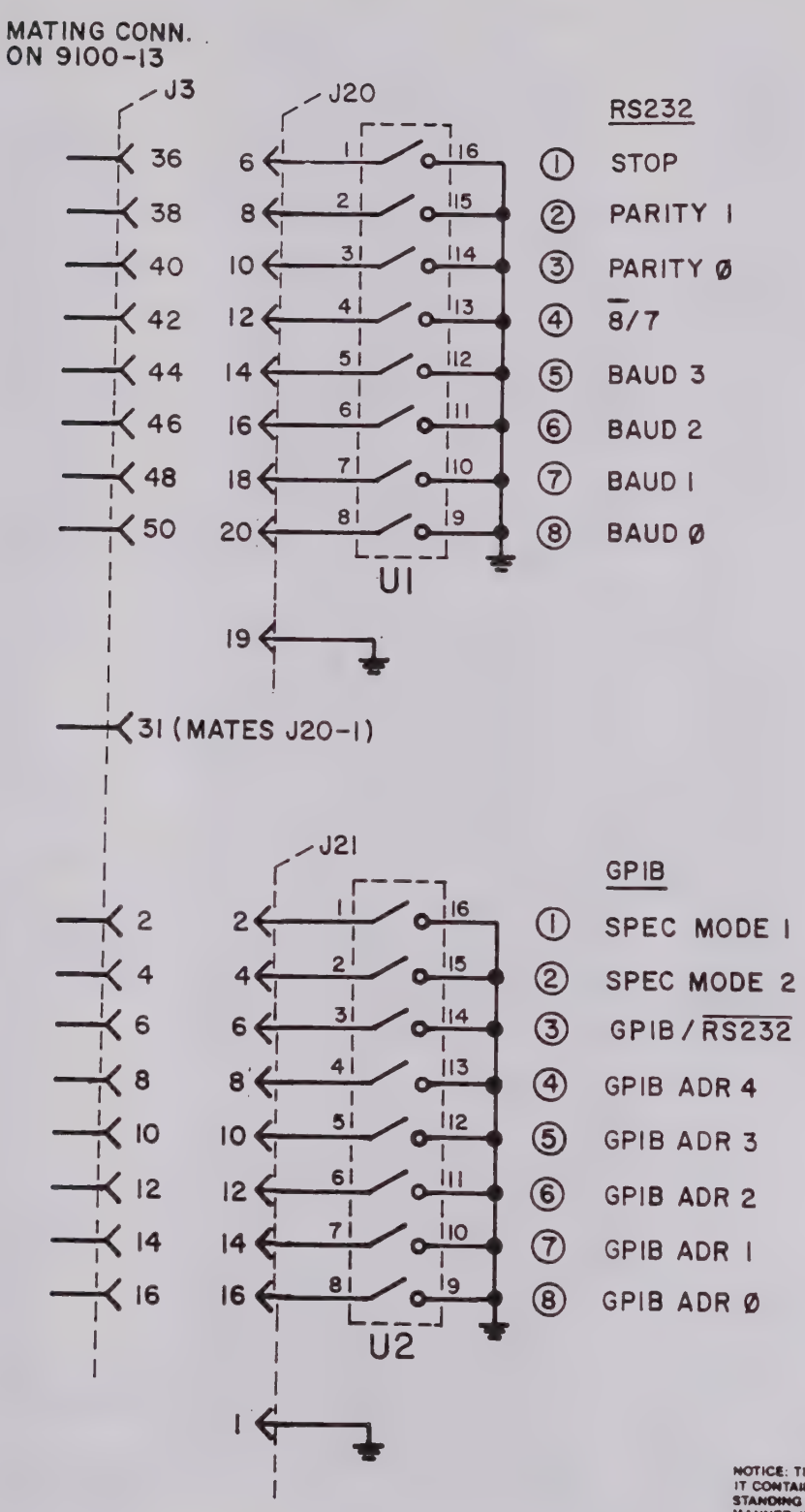
LeCroy RESEARCH SYSTEMS

ELECTRONIC SCHEMATIC
9100-4
BACKPLANE BOARD

9100-4-81

LAST REFERENCE DESIGNATION USED
C10 J6 A6 P1 U9 R6

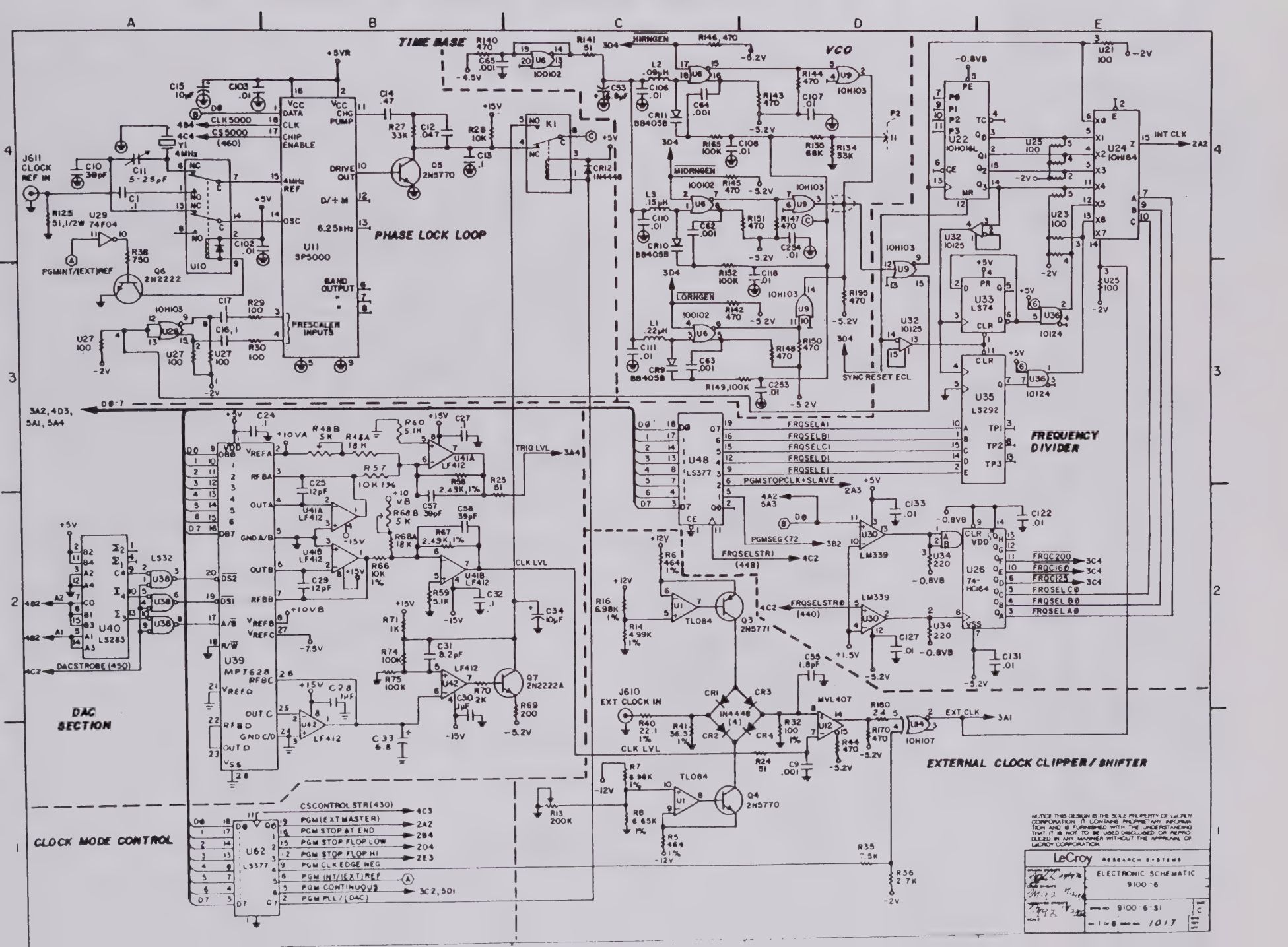
NOTE UNLESS OTHERWISE SPECIFIED.
ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 5%.
ALL CAPACITOR VALUES ARE IN MICROFARADS

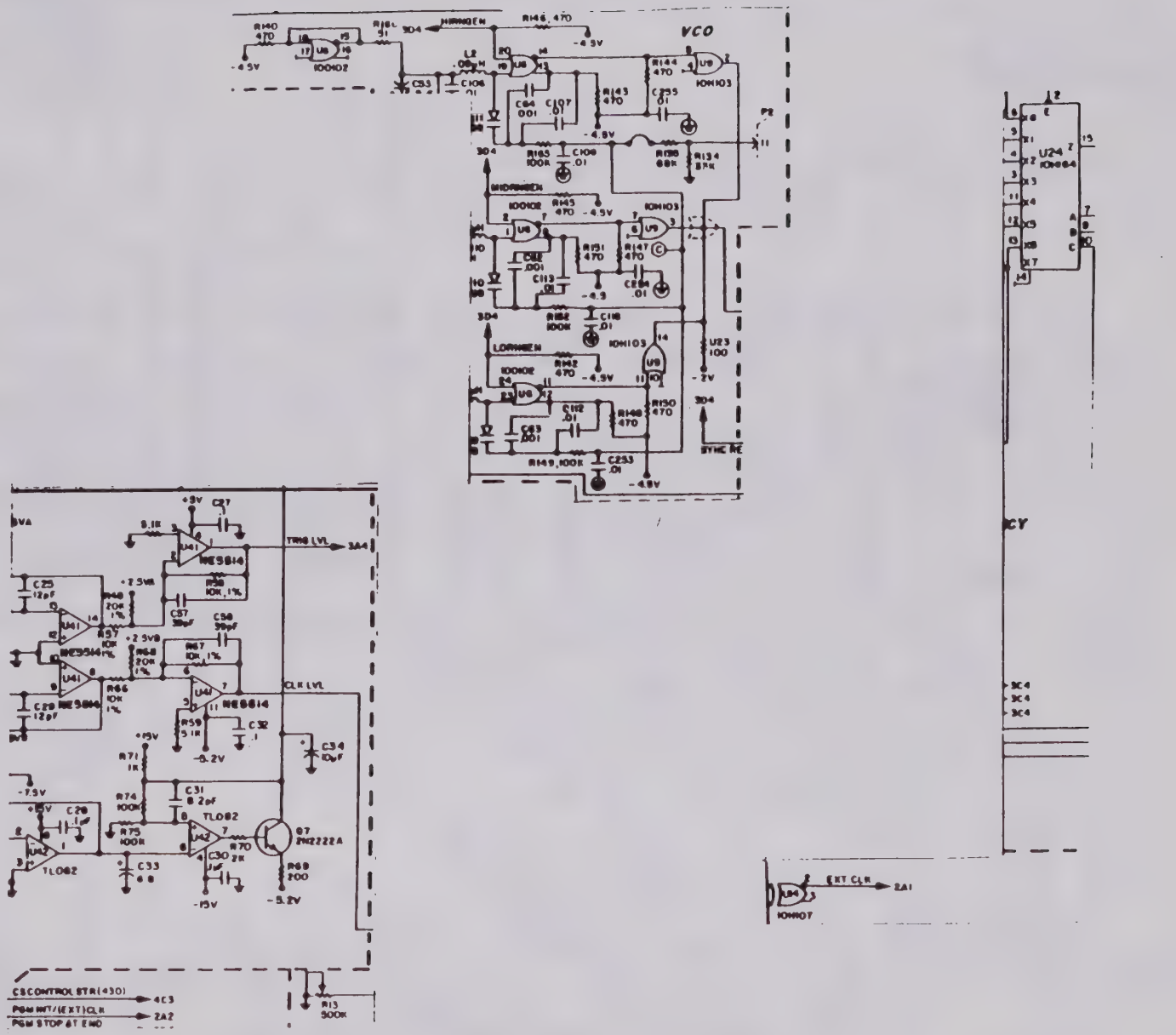


NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LeCROY RESEARCH SYSTEMS IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDER STANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCROY RESEARCH SYSTEMS

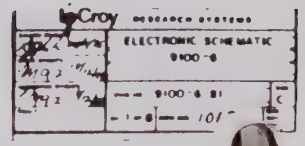
LeCroy RESEARCH SYSTEMS

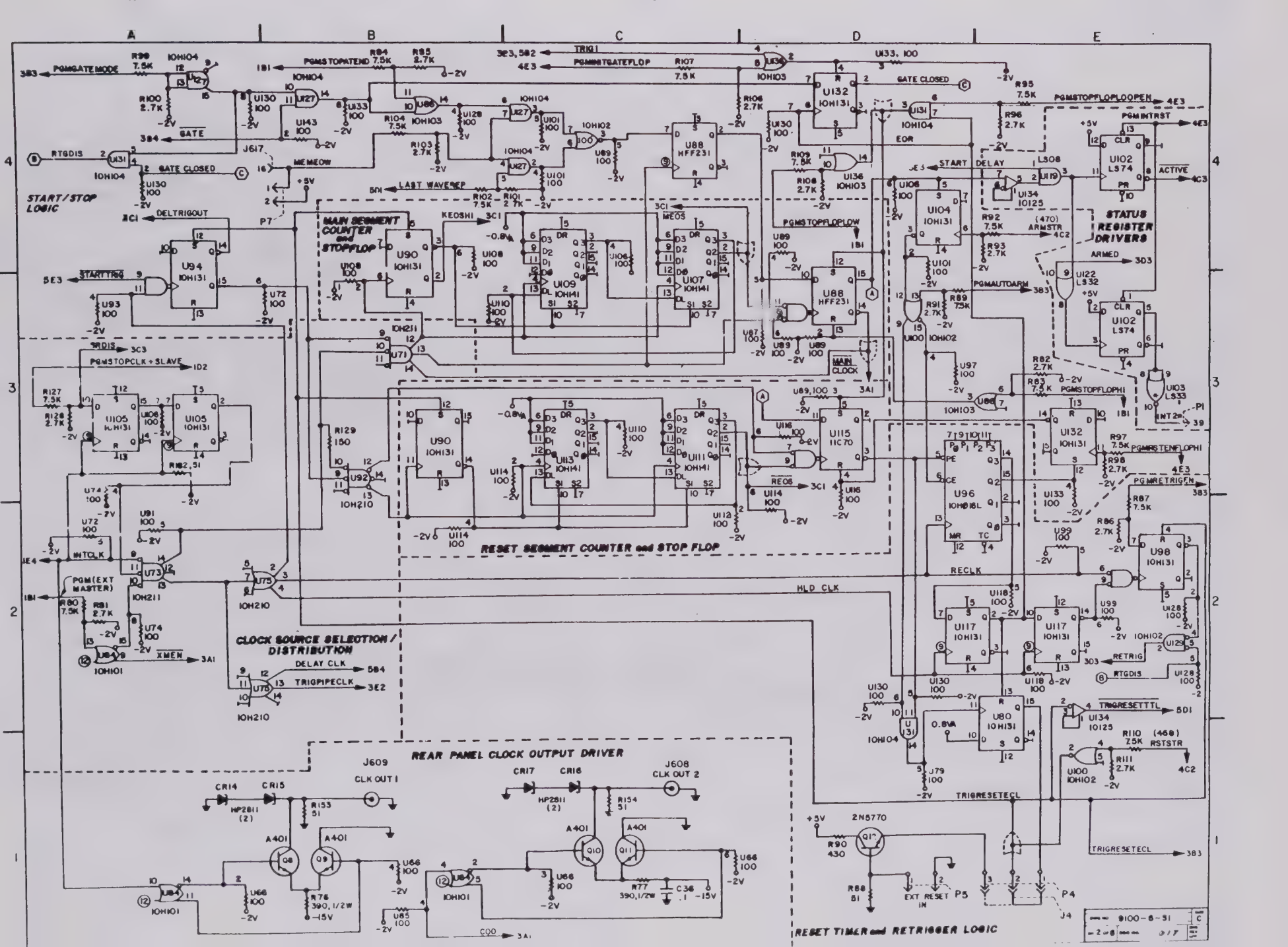
DRAWN BY/DATE	ELECTRICAL SCHEM
CHKD BY/DATE	9100-5
APPROVED BY/DATE	DWG NO: 9100-S1 SIZ A
SCALE	SH. 1 OF 1 ECO NO. 1001 ENG REV APP


TIME BASE
PHASE LOCK LOOP
VCO
FREQUENCY DIVIDER
DAC SECTION
CLOCK MODE CONTROL
EXTERNAL CLOCK CLIPPER/SHIFTER
J611 CLOCK REF IN
U11 SP9000
U10
U29 74F04
U40 LS283
U39 MP7628
U62 LS377
U48 LS377
U35 LS292
U22 10H016L
U24 10H164
U26 74-HC164
U33 LS74
U30 LM339
U34 220
U36 10124
U32 10125
U23 100
U25 100
U21 100
U27 100
U38 LS32
U41A LF412
U41B LF412
U42 LF412
U1 TL084
Q1 2N5770
Q3 2N5771
Q4 2N5770
Q7 2N2222A
Q6 2N2222
U6 100102
U9 10H103
U12 MVL407
U4 10H107
K1
CR1 BB405B
CR2 BB405B
CR9 BB405B
CR10 BB405B
CR11 BB405B
CR12 1N4448
CR1 IN4448 (4)
J610 EXT CLOCK IN
INT CLK
EXT CLK
FRQSELA!
FRQSELB!
FRQSELC!
FRQSELD!
FRQSELE!
PGMSTOPCLK+SLAVE
PGMSEG<72
FRQSELSTR!
FRQSELSTR0
FRQC200
FRQC160
FRQC125
FRQSEL C0
FRQSEL B0
FRQSEL A0
SYNC RESET ECL
DACSTROBE(450)
CSCONTROLSTR(430)
PGM(EXT MASTER)
PGM STOP AT END
PGM STOP FLOP LOW
PGM STOP FLOP HI
PGM CLK EDGE NEG
PGM INT/(EXT)REF
PGM CONTINUOUS
PGM PLL/(DAC)
HIRNGEN
MIDRNGEN
LORNGEN
TRIG LVL
CLK LVL
LeCroy RESEARCH SYSTEMS
ELECTRONIC SCHEMATIC
9100-6
9100-6-SI
1017

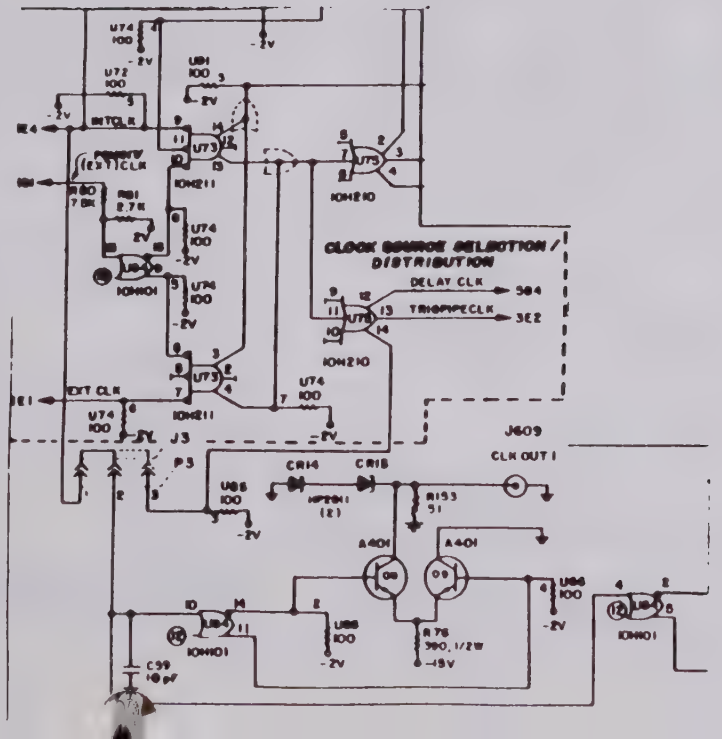


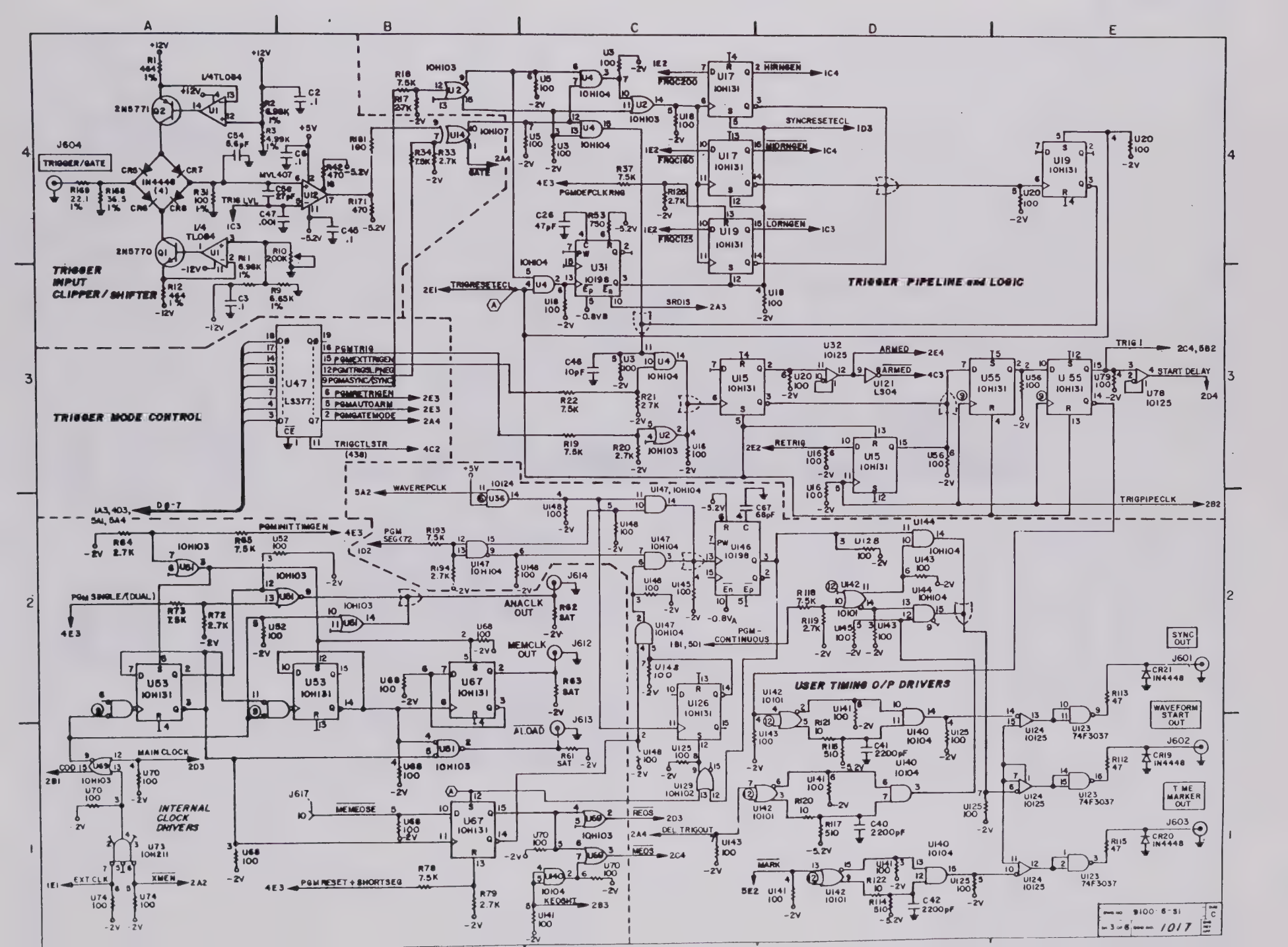
NOTE: THIS PAGE OF SCHEMATIC REFLECTS CONNECTIONS FOR REV. E AND EARLIER 9100-6 BOARDS ONLY.



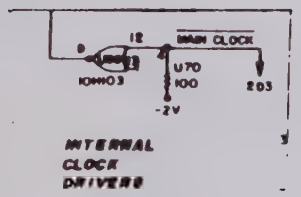

START/STOP LOGIC
MAIN SEGMENT COUNTER and STOPFLOP
RESET SEGMENT COUNTER and STOP FLOP
CLOCK SOURCE SELECTION / DISTRIBUTION
REAR PANEL CLOCK OUTPUT DRIVER
RESET TIMER and RETRIGGER LOGIC
STATUS REGISTER DRIVERS
PGMGATEMODE
PGMSTOPATEND
PGMSTOPGATEFLOP
TRIG1
GATE CLOSED
EOR
START
DELAY
ACTIVE
ARMED
PGMAUTOARM
PGMINTRST
PGMSTOPFLOPLOOPEN
PGMSTOPFLOPLOW
PGMSTOPFLOPHI
PGMRSTENFLOPHI
PGMRETRIGEN
DELTRIGOUT
STARTTRIG
LAST WAVEREP
MEMEOW
KEOSHI
MEOS
REOS
MAIN CLOCK
PGMSTOPCLK + SLAVE
INTCLK
PGM(EXT MASTER)
XMEN
DELAY CLK
TRIGPIPECLK
HLD CLK
RECLK
RETRIG
RTGDIS
TRIGRESETTTL
TRIGRESETECL
CLK OUT 1
CLK OUT 2
EXT RESET IN
2N5770
HP2811 (2)
A401
U132 10H131
U104 10H131
U88 HFF231
U107 10H141
U109 10H141
U90 10H131
U96 10H016L
U115 11C70
U117 10H131
U80 10H131
U98 10H131
U102 LS74
U103 LS33
U122 LS32
U134 10125
U100 10H102
U105 10H131
U71 10H211
U92 10H210
U73 10H211
U76 10H210
U94 10H131
U93 100
U72 100
U74 100
U91 100
U80 10H101
U66 100
U65 100
U67 100
U68 100
U69 100
U70 100
U87 100
U89 100
U97 100
U99 100
U118 100
U128 100
U129 100
U130 100
U131 100
U133 100
U134 100
U135 100
U136 10H103
U137 10H104
U138 10H102
U139 10H104
U140 10H104
U141 10H104
U142 10H104
U143 100
R99 7.5K
R100 2.7K
R104 7.5K
R103 2.7K
R102 7.5K
R101 2.7K
R106 2.7K
R107 7.5K
R108 2.7K
R109 7.5K
R95 7.5K
R96 2.7K
R92 7.5K
R93 2.7K
R91 2.7K
R89 7.5K
R82 2.7K
R83 7.5K
R97 7.5K
R98 2.7K
R87 7.5K
R86 2.7K
R84 7.5K
R85 2.7K
R127 7.5K
R128 2.7K
R129 180
R82,51
R80 7.5K
R81 2.7K
R110 (468) 7.5K RSTSTR
R111 2.7K
R153 51
R154 51
R77 390, 1/2W
C36 .1 -15V
R90 430
R88 51
J609
J608
J617
P1
P4
P5
P7
J4
CR14
CR15
CR16
CR17
Q8
Q9
Q10
Q11
Q12
C00
9100-6-51

NOTE: THIS PAGE OF SCHEMATIC REFLECTS CONNECTIONS FOR REV. E AND EARLIER 9100-6 BOARDS ONLY.

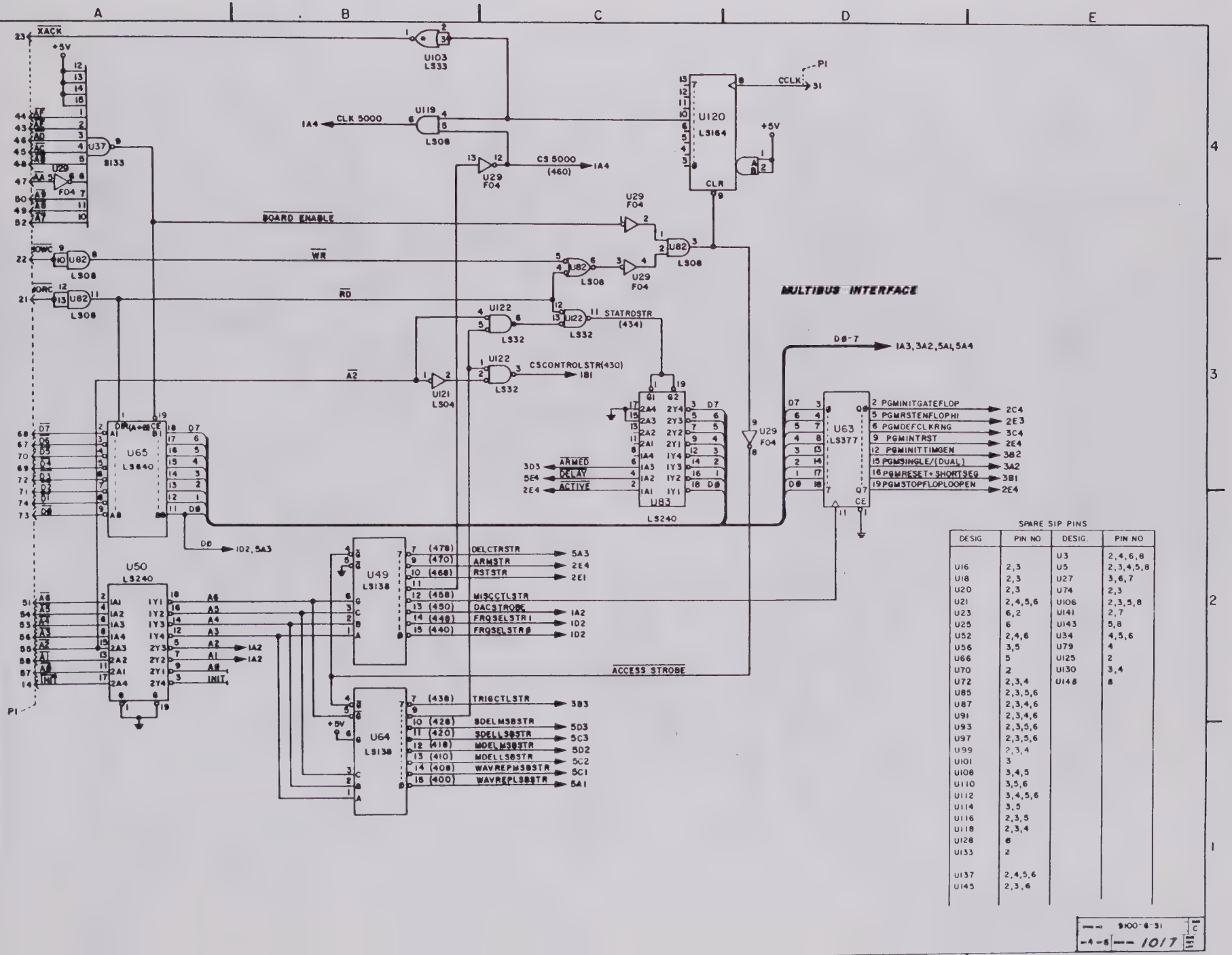



TRIGGER INPUT CLIPPER/SHIFTER
TRIGGER MODE CONTROL
TRIGGER PIPELINE and LOGIC
USER TIMING O/P DRIVERS
INTERNAL CLOCK DRIVERS
TRIGGER/GATE
TRIG LVL
TRIGCTLSTR (43B)
TRIGRESETECL
SRDIS
PGMDEPCLKRNG
SYNCRESETECL
HIRNGEN
MIDRNGEN
LORNGEN
ARMED
RETRIG
TRIG!
START DELAY
TRIGPIPECLK
WAVEREPCLK
PGMINITTRIGEN
PGM SINGLE/(DUAL)
PGM-CONTINUOUS
ANACLK OUT
MEMCLK OUT
ALOAD
MAIN CLOCK
MEMEOSE
REOS
MEOS
DEL TRIGOUT
KEOSHT
EXT CLK
XMEN
PGM RESET + SHORTSEG
MARK
SYNC OUT
WAVEFORM START OUT
TIME MARKER OUT
9100-6-31
1017

NOTE: THIS PAGE OF SCHEMATIC REFLECTS CONNECTIONS FOR REV. E
AND EARLIER 9100-6 BOARDS ONLY.

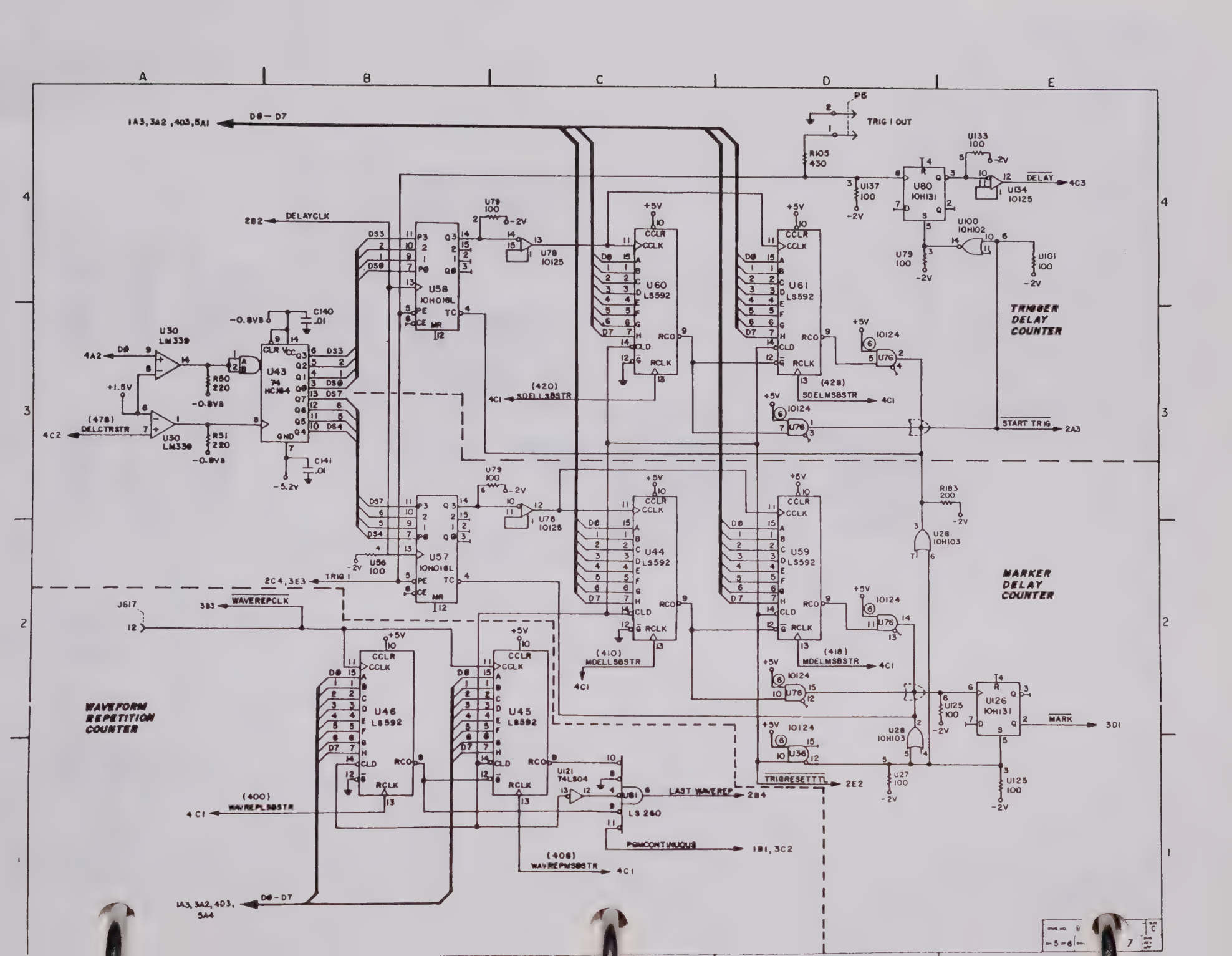


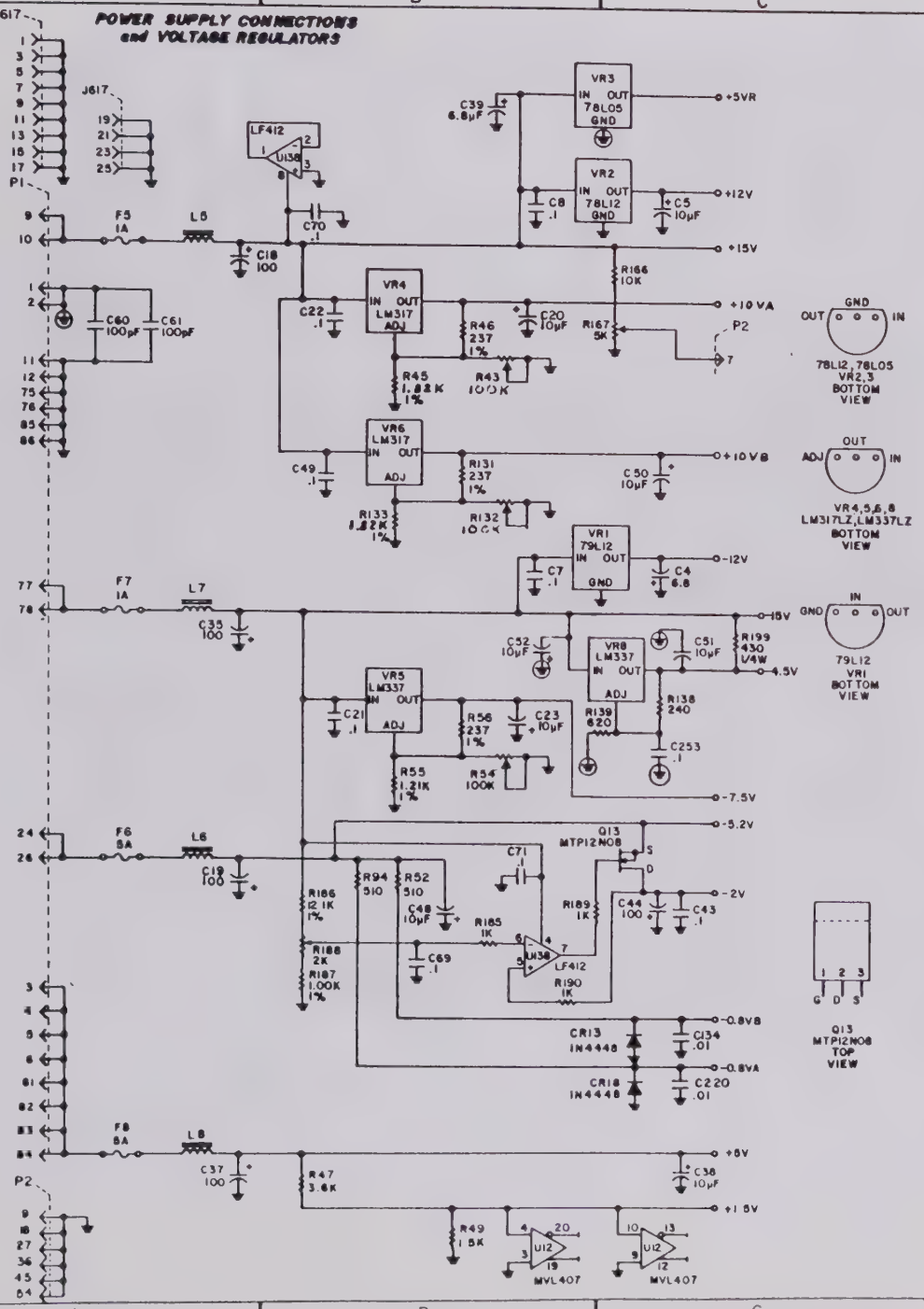
INTERNAL
CLOCK
DRIVERS



SPARE SIP PINS

DESIG	PIN NO	DESIG.	PIN NO
		U3	2,4,6,8
U16	2,3	U5	2,3,4,5,8
U18	2,3	U27	3,6,7
U20	2,3	U74	2,3
U21	2,4,5,6	U106	2,3,5,8
U23	6,2	U141	2,7
U25	6	U143	5,8
U52	2,4,6	U34	4,5,6
U56	3,5	U79	4
U66	5	U125	2
U70	2	U130	3,4
U72	2,3,4	U148	8
U85	2,3,5,6		
U87	2,3,4,6		
U91	2,3,4,6		
U93	2,3,5,6		
U97	2,3,5,6		
U99	2,3,4		
U101	3		
U108	3,4,5		
U110	3,5,6		
U112	3,4,5,6		
U114	3,5		
U116	2,3,5		
U118	2,3,4		
U128	6		
U133	2		
U137	2,4,5,6		
U145	2,3,6		


TRIGGER DELAY COUNTER
MARKER DELAY COUNTER
WAVEFORM REPETITION COUNTER
TRIG I OUT
DELAY
START TRIG
MARK
TRIGRESETTTL
LAST WAVEREP
PGMCONTINUOUS
DELAYCLK
WAVEREPCLK
SDELLSBSTR
SDELMSBSTR
MDELLSBSTR
MDELMSBSTR
WAVREPLSBSTR
WAVREPMSBSTR
U60 LS592
U61 LS592
U44 LS592
U59 LS592
U46 LS592
U45 LS592
U58 10H016L
U57 10H016L
U43 74HC164
U30 LM339
U30 LM336
U80 10H131
U126 10H131
U28 10H103
U76 10124
U78 10125
U134 10125
U121 74LS04
U81 LS 260
U100 10H102
U133 100
U79 100
U86 100
U125 100
U27 100
U137 100
U101 100
R105 430
R183 200
R50 220
R51 220
C140 .01
C141 .01
-0.8V8
-5.2V
+1.5V
+5V
-2V
D0 – D7
1A3, 3A2, 4D3, 5A1
1A3, 3A2, 4D3, 5A4
2B2
4A2
4C2
4C1
2C4, 3E3
3B3
J617
2B4
1B1, 3C2
2E2
3D1
(420)
(428)
(478)
(410)
(418)
(400)
(408)



VOLTAGE AND GND PIN NUMBERS

DEVICE	REF. DESIGNATION	-4.5V	+15V	+5V	GRD	-0.8V	-5.2V	-15V	+12V	-12V
10HI01	U84				1,16		8			
10HI02	U100, 129				1,16		8			
10HI03	U2, 28, 51, 69, 86, 136, 9				1,16		8			
10HI04	U4, 127, 131, 144, 147				1,16		8			
10HI07	U14				1,16		8			
10HO16L	U22, 57, 58, 96				1,16		8			
10HI31	U15, 17, 19, 53, 55, 67, 80, 90 94, 98, 104, 117, 126, 132, 105				1,16		8			
10HI41	U107, 109, 111, 113				1,16		8			
10HI64	U24				1,16		8			
10H210	U75, 92				1,16		8			
10H211	U71, 73				1,16		8			
74LS08	U82, 119			14	7					
74LS32	U38, 122			14	7					
74LS33	U103			14	7					
74LS74	U33, 102			14	7					
74LSI38	U49, 64			16	8					
74LS240	U50, 83			20	10					
74LS260	U81			14	7					
74LS283	U40			16	8					
74LS292	U35			16	8					
74LS377	U47, 48, 62, 63			20	10					
74LS592	U44, 45, 46, 59, 60, 61			16	8					
74LS640	U65			20	10					
74LS164	U120			14	7					
74S133	U37			16	8					
74HC164	U26, 43					14	7			
74F04	U29			14	7					
10124	U36, 76			9	16		8			
10125	U32, 78, 124, 134			9	16		8			
10198	U31, U146				1,16		8			
SP5000	U11			16,2	5,9					
MVL407	U12			2	1,16		11			
MP7628	U39			1	28					
LM339	U30			3			12			
74LS04	U121			14	7					
100102	U6	21			9,10					
10104	U140				1,16		8			
10101	U142				1,16		8			
LF412	U136, 41A, 41B, 42		8					4		
TL084	U1								4	11
74F3037	U123			12,13	4,5					
HFF131	U88				1,16		8			
11C70	U115				1,16		8			

SPARE GATE PINS & CHIPS

REF. DESIG.	PIN NUMBERS	REF DESIG.	PIN NUMBERS
U2	3,6,7	U103	4,5,6; 11,12,13
U123	6,7,8	U71	2,3,4,5,6,7
U28	10,11,14	U78	5,6
U32	8,7	U104	10,11,12,13,14,15
U38	11,12,13	U144	2,4,5; 3,6,7
U33	8,9,10,11,12,13	U119	8,9,10; 11,12,13
U149	ALL	U121	3,4,5,6; 10,11
U150	ALL	U124	2,3,4
U14	12,13,14,15	U129	3,6,7; 10,11,14
U147	ALL	U134	13,14,15
U81	1,2,3,12,13,5	U136	3,6,7, 12,13,15,9
U84	3,6,7	U140	2,4,5
U92	2,3,4,5,6,7	U6	3,4,5 6
U148	ALL		
U131	12,13,15,9	U86	2,4,5; 9,12,13,15

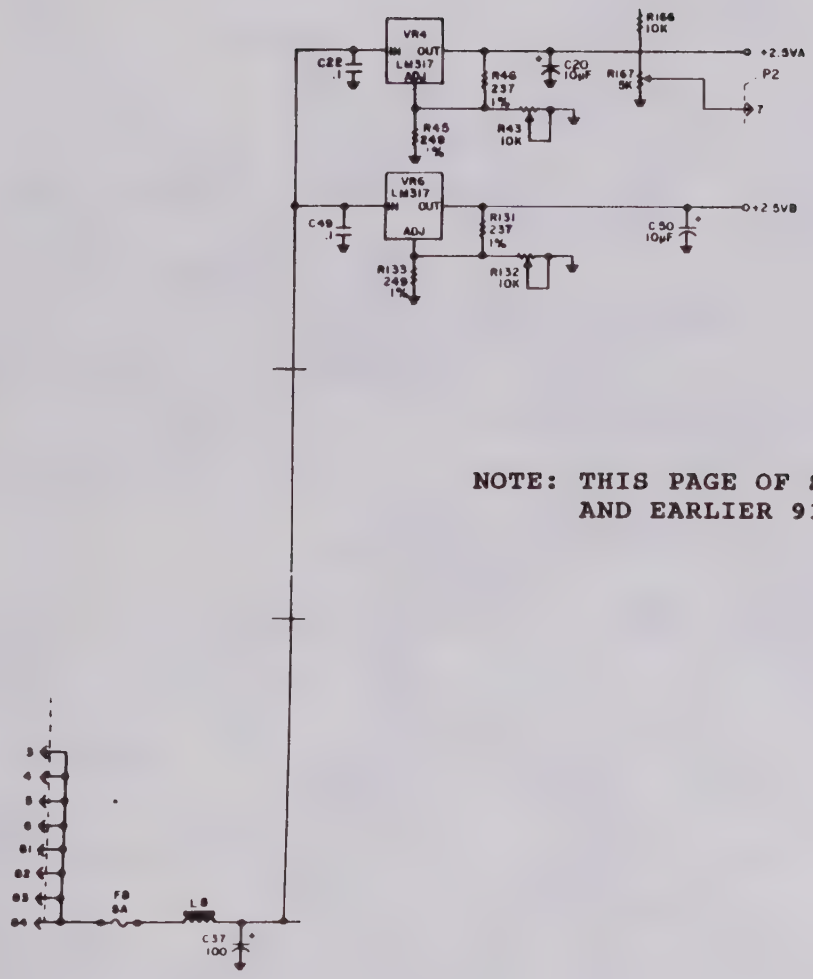
LAST REFERENCE DESIGNATION USED

Z	R	L	F	U	Q	N	J	Y	W	T	P	VR
200	200	8	8	136	13	1	1	1	1	4	7	7

NOTE UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

9100-8-31 C

1017



NOTE: THIS PAGE OF SCHEMATIC REFLECTS CONNECTIONS FOR REV. E AND EARLIER 9100-6 BOARDS ONLY.

9100-6 Acronym Dictionary

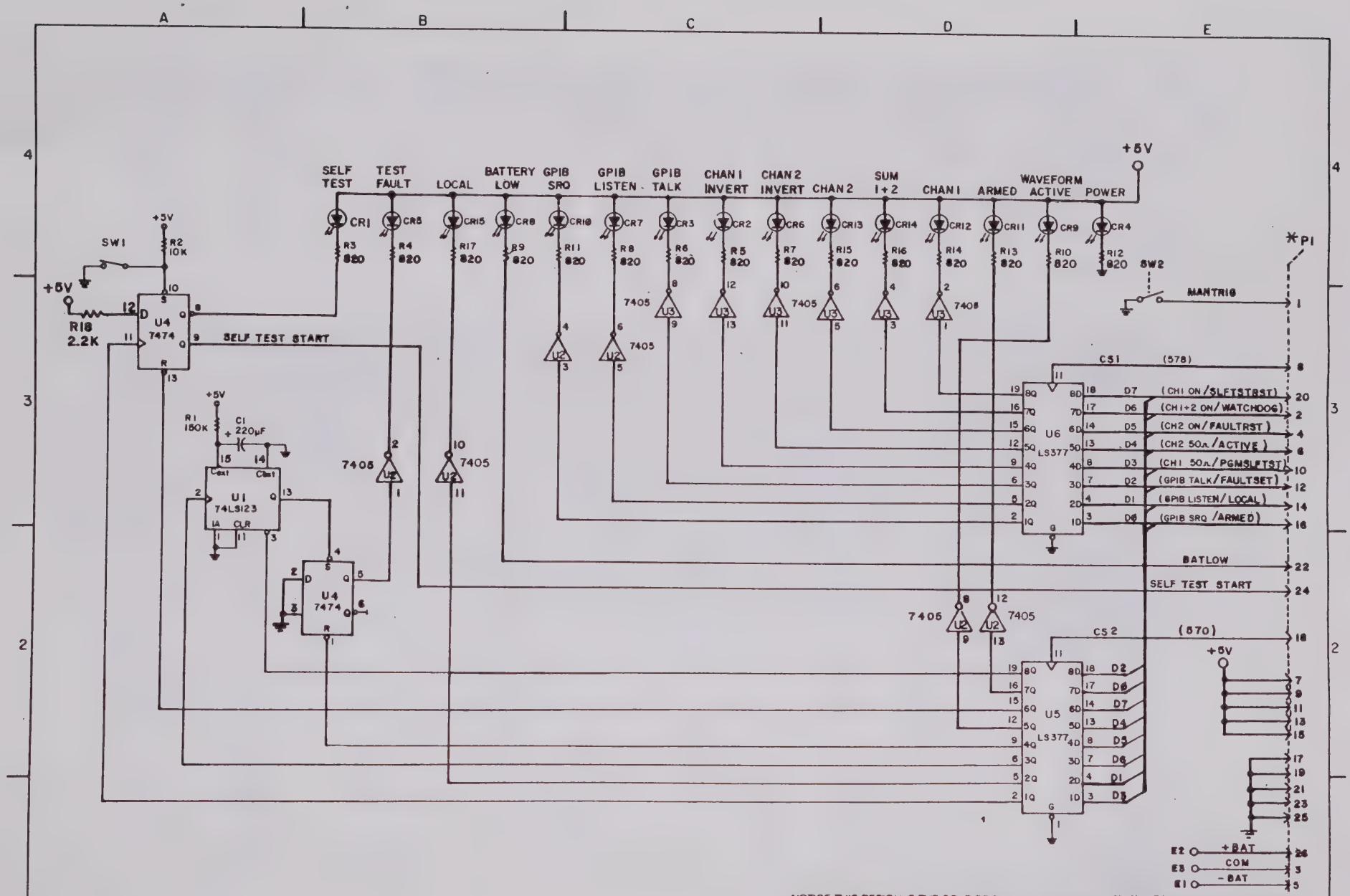
Acronym	Definition
A0-AF	multibus Address signals
ACTIVE	The AFG is Active
ANACLK OUT	Analog Clock Output (to -2)
ARMED	the trigger is Armed
ARMSTR(470)	Arming Strobe (address 470)
CCLK	multibus Clock "C" signal
CLK5000	Data Clock for SP5000
CLKLVL	external Clock input threshold Level
COD	Clock Output Driver
CS5000	Chip Select for SP5000
CSCONTROLSTR(430)	Clock & Stop logic Control Strobe (address 430)
D0	Data Bit 0
D0-7	Data bus bits 0 - 7
DACSTROBE(450)	DAC select Strobe (address 450)
DELAY	start Delay is being counted through
DELAYCLK	trigger & marker Delay counter Clock
DELCTRSTR(478)	Delay Counters least significant bits Strobe (address 478)
DELTRIGOUT	Delayed Trigger (Start) Output driver
EOWE	End Of Waveform (ECL level)
EXT CLOCK IN	External Clock Input (Rear Panel)
EXT RESET IN	External trigger Reset Input
EXTCLK	External Clock
FRQSELA0-C0	Frequency Selection Bits A0 - C0
FRQSELA1-E1	Frequency Selection Bits A1 - E1
FRQSELSTR0(440)	Frequency Selection Strobe 0 (Address 440)
FRQSELSTR1(448)	Frequency Selection Strobe 1 (Address 448)
GATE	the Gate signal
GATECLOSED	the Gate is inactive (i.e. Closed)
HI,MID,LORNGEN	Enables for High, Middle, & Low Range VCOs
HLDCLK	trigger reset & retrigger Holdoff Clock
INIT	multibus Initialize signal
INTCLK	Internal Clock
IORC	multibus I/O Read Command
IOWC	multibus I/O Write Command
KEOSHI	Keep End-Of-Segment Hi
LASTWAVEREP	Last Waveform Repetition
LOAD	Analog Load output (to -2)
MAINCLOCK	Main Clock to internal Clock drivers
MARK	Marker out driver
MDELLSBSTR(410)	Marker Delay counter Less Significant Byte Strobe (address 410)
MDELMSBSTR(418)	Marker Delay counter Most Significant Byte Strobe (address 418)
MEMCLK OUT	Memory Clock Output (to 9100-1)
MEMEOSE	End-Of-Segment (ECL level) from Memory (9100-1)
MEMEOW	End Of Waveform from Memory (9100-1)
MEOS	Main stop flop's End Of Segment

9100-6 Acronym Dictionary

Acronym	Definition
MISCCTLSTR(458)	Miscellaneous Control Strobe (address 458)
PGMASYNC/(SYNC)	Program Asynchronous or Synchronous trigger mode
PGMAUTOARM	Program Automatic re-Arming
PGMCLKEDGENEG	Program external Clock Edge Negative
PGMCONTINUOUS	Program Continuous mode
PGMDEFCLKRNG	Program Default Clock Range
PGM(EXTMASTER)	Program External Master clock source
PGMEXTTRIGEN	Program External Trigger Enable
PGMGATEMODE	Program for Gate Mode
PGMINITGATEFLOP	Program Initialize Gate holdoff Flop
PGMINITTIMGEN	Program Initialize Timing output Generator
PGMINT/(EXT)REF	Program Internal or External PLL Reference
freq. PGMINTRST	Program Interrupt Reset
PGMPLL/(DAC)	Program Phase-Lock Loop or DAC for VCO control
PGMRESET+SHORTSEG	Program Reset or Short Segment
PGMRETRIGEN	Program Retrigger Enable
PGMRSTENFLOPHI	Program Reset Enable Flop High
PGMSEG<72	Program for Segment length less than 72 bytes long
PGMSINGLE/(DUAL)	Program Single or Dual output mode
PGMSTOPATEND	Program Stop At next End of waveform
PGMSTOPCLK+SLAVE	Program Stop Clock or Slave Mode
PGMSTOPFLOPHI	Program Stop Flop High
PGMSTOPFLOPLOOPEN	Program Stop Flop Loop Enable
PGMSTOPFLOPLOW	Program Stop Flop Low
PGMTRIG	Program Trigger
PGMTRIGSLPNEG	Program external Trigger Slope Negative
RD	Read
RECLK	Reset timer & Retrigger Clock
REOS	Reset stop flop's End Of Segment
RETRIG	Retrigger
RSTSTR(468)	trigger Reset Strobe (address 468)
RTGDIS	Retrigger Disable
SDELLSBSTR(420)	Start Delay counter Less Significant Byte Strobe (address 420)
SDELMSBSTR(428)	Start Delay counter Most Significant Byte Strobe (address 428)
SRDIS	Synchronous Reset Disable
STARTDELAY	beginning of Start Delay period
STARTTRIG	Start Trigger
STATRDSTR(434)	Status register Read Strobe (address 434)
SYNCRESETECL	Reset for Synchronous trigger circuitry (ECL level)
TRIG1	Trigger # 1
TRIGCTLSTR(438)	Trigger Control Strobe (address 438)
TRIGGER/GATE	External Trigger or Gate input
TRIGLVL	external Trigger input threshold Level

9100-6 Acronym Dictionary

Acronym	Definition
TRIGPIPECLK	Trigger Pipeline Clock
TRIGRESETECL	Trigger Reset (ECL level)
TRIGRESETTTL	Trigger Reset (TTL Level)
WAVEREPCLK	Waveform Repetition Clock
WAVREPLSBSTR(400)	Waveform Repetition counter Less Significant
Byte	Strobe (address 400)
WR	Write
XACK	multibus Acknowledge signal
XMEN	External Master Enable



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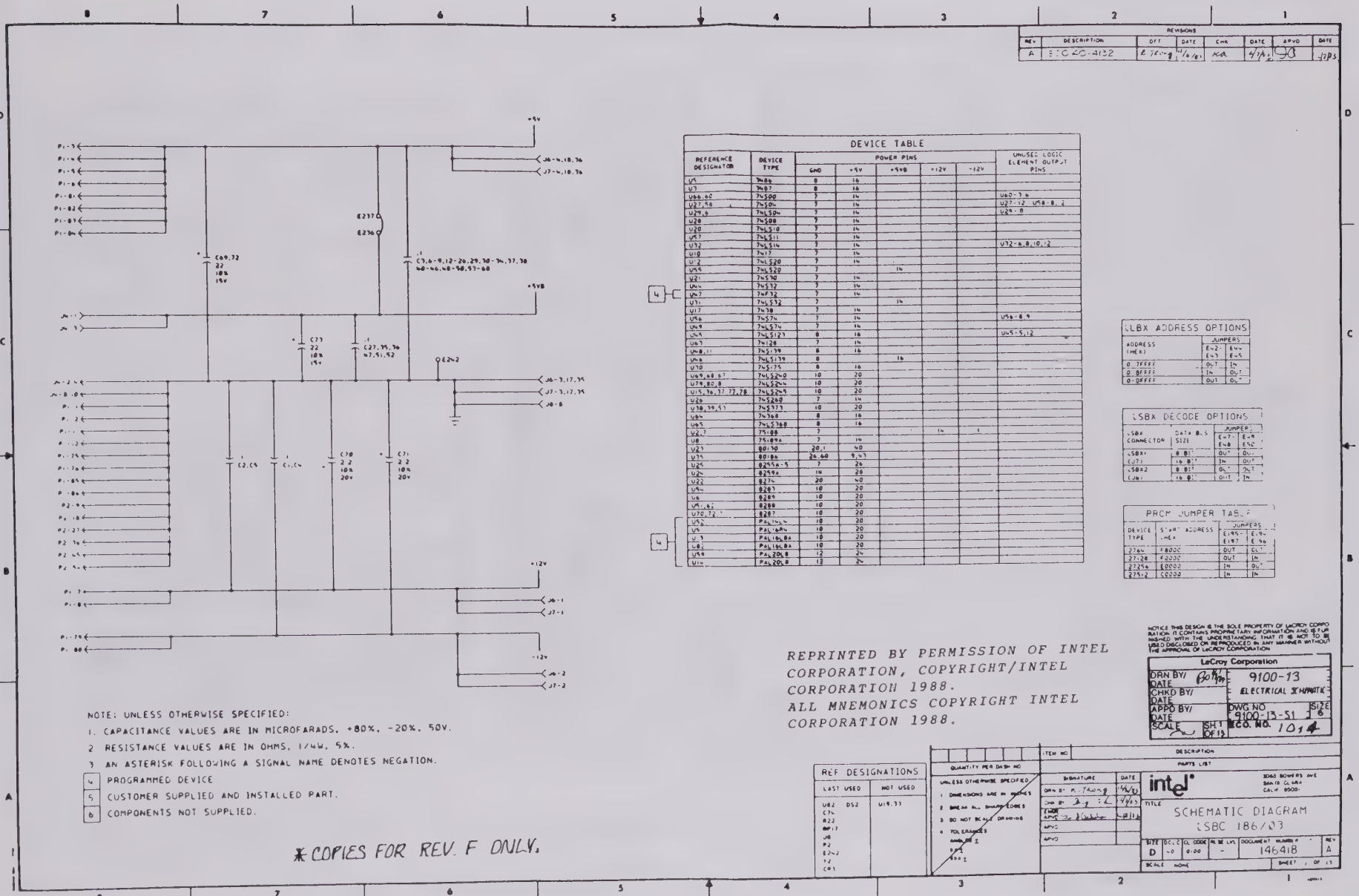
LAST REFERENCE DESIGNATION USED						
U6	CR15	R18	SW2	P1		

NOTE UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE IN OHMS 1/8W 5%
ALL CAPACITOR VALUES ARE IN MICROFARADS

LeCroy RESEARCH SYSTEMS

9100-7
FRONT PANEL
ELECTRICAL SCHEMATIC


REVISIONS
REV | DESCRIPTION | DFT | DATE | CHK | DATE | APVD | DATE
A | ECO 20-4132 | R TRAN | 11/6/81 | KA | 4/1/82 | JB | 4/7/82
DEVICE TABLE
REFERENCE DESIGNATOR | DEVICE TYPE | POWER PINS: GND | +5V | +5VB | +12V | -12V | UNUSED LOGIC ELEMENT OUTPUT PINS
LSBX ADDRESS OPTIONS
ADDRESS (HEX) | JUMPERS: E4-2 | E4-3 | E4-4 | E4-5
0-7EFFF | OUT | IN | OUT | IN
0-BFFFF | IN | OUT | IN | OUT
0-DFFFF | OUT | IN | OUT | OUT
LSBX DECODE OPTIONS
LSBX CONNECTOR | DATA BUS SIZE | JUMPER: E4-7 | E4-8 | E4-9 | E4-10
LSBX1 (J7) | 8 BIT | OUT | IN | OUT | OUT
LSBX1 (J7) | 16 BIT | IN | OUT | OUT | IN
LSBX2 (J8) | 8 BIT | OUT | IN | OUT | OUT
LSBX2 (J8) | 16 BIT | IN | OUT | IN | IN
PROM JUMPER TABLE
DEVICE TYPE | START ADDRESS (HEX) | JUMPERS: E1-95 - E1-97 | E1-96
2764 | E000 | OUT | OUT
27128 | C000 | OUT | IN
27256 | 8000 | IN | OUT
27512 | 0000 | IN | IN
NOTE: UNLESS OTHERWISE SPECIFIED:
1. CAPACITANCE VALUES ARE IN MICROFARADS, +80%, -20%, 50V.
2 RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
3 AN ASTERISK FOLLOWING A SIGNAL NAME DENOTES NEGATION.
4 PROGRAMMED DEVICE
5 CUSTOMER SUPPLIED AND INSTALLED PART.
6 COMPONENTS NOT SUPPLIED.
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LeCroy Corporation
DRN BY/ DATE
CHKD BY/ DATE
APPD BY/ DATE
SCALE
9100-13
ELECTRICAL SCHEMATIC
DWG NO 9100-13-S1
SIZE D
ECO NO. 1014
SHT OF 13
REF DESIGNATIONS
LAST USED | NOT USED
U82 D52 | U19,33
C74
R22
RP17
J8
P2
E2-2
Y2
CR1
UNLESS OTHERWISE SPECIFIED
1 DIMENSIONS ARE IN INCHES
2 BREAK ALL SHARP EDGES
3 DO NOT SCALE DRAWING
4 TOLERANCES
ITEM NO | DESCRIPTION | QUANTITY PER DASH NO
PARTS LIST
SIGNATURE | DATE
DRN BY R. TRAN 4/6/82
CHK BY J.J. 4/7/82
ENGR
APVD
APVD
intel
3065 BOWERS AVE
SANTA CLARA
CALIF 95051
TITLE
SCHEMATIC DIAGRAM
iSBC 186/03
SIZE D | DOC. CONT. -00 | CL CODE 0100 | REV LTR - | DOCUMENT NUMBER 146418 | REV A
SCALE NONE
SHEET 1 OF 13

Figure 5-2. Schematic Diagram (Sheet 1 of 13)

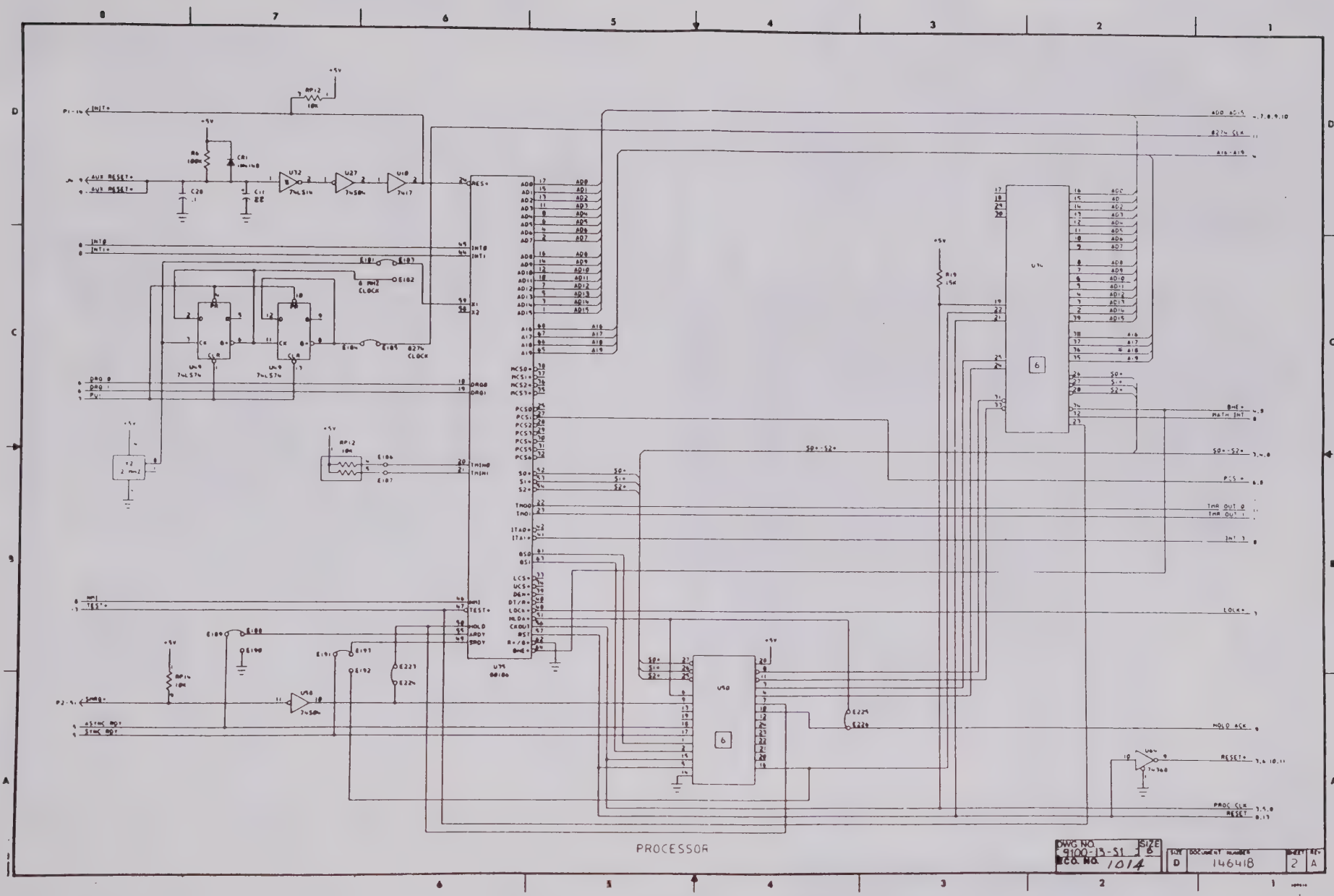

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Figure 5-2. Schematic Diagram (Sheet 2 of 13)

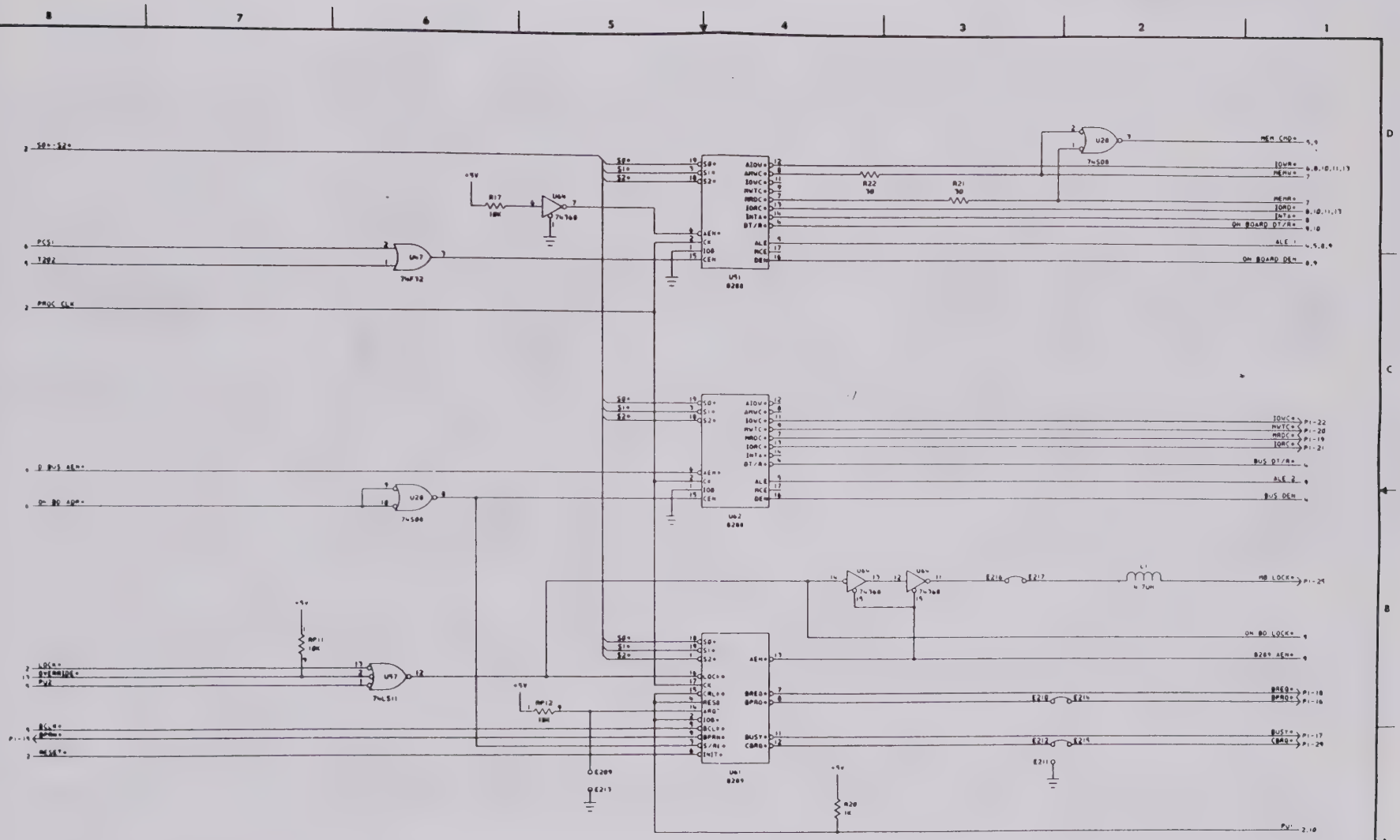

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Figure 5-2. Schematic Diagram (Sheet 3 of 13)

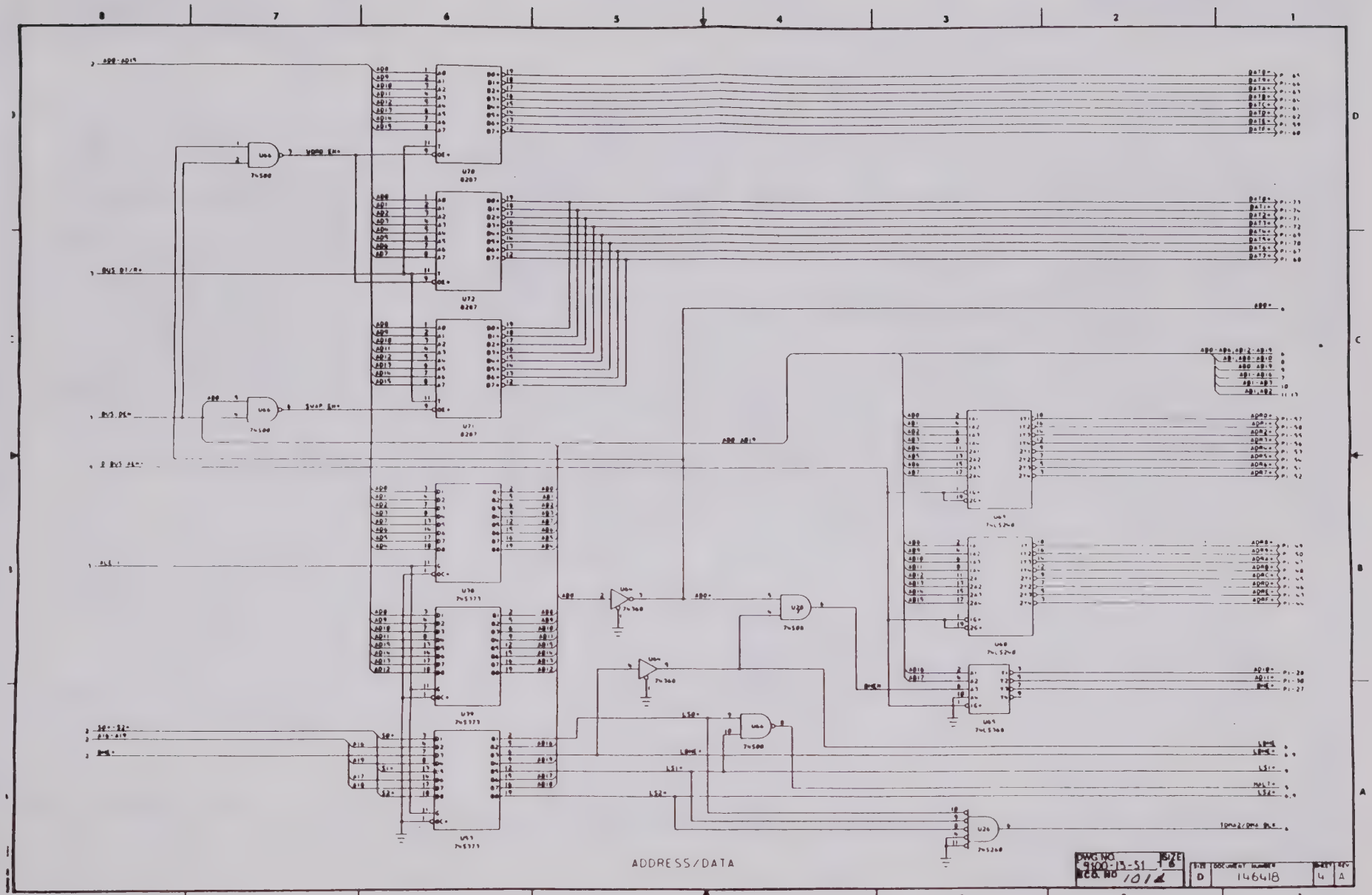

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Figure 5-2. Schematic Diagram (Sheet 4 of 13)

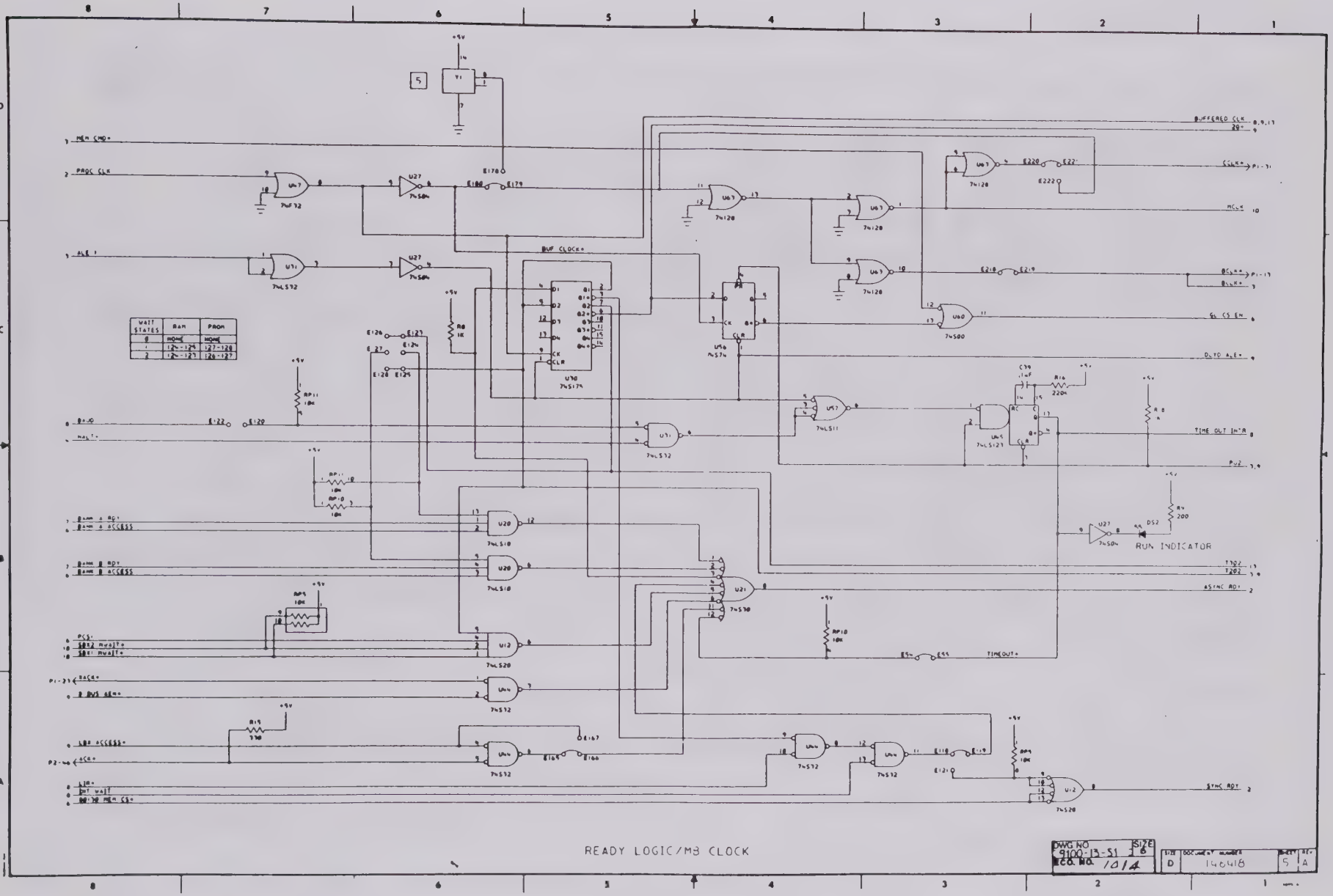

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Figure 5-2. Schematic Diagram (Sheet 5 of 13)

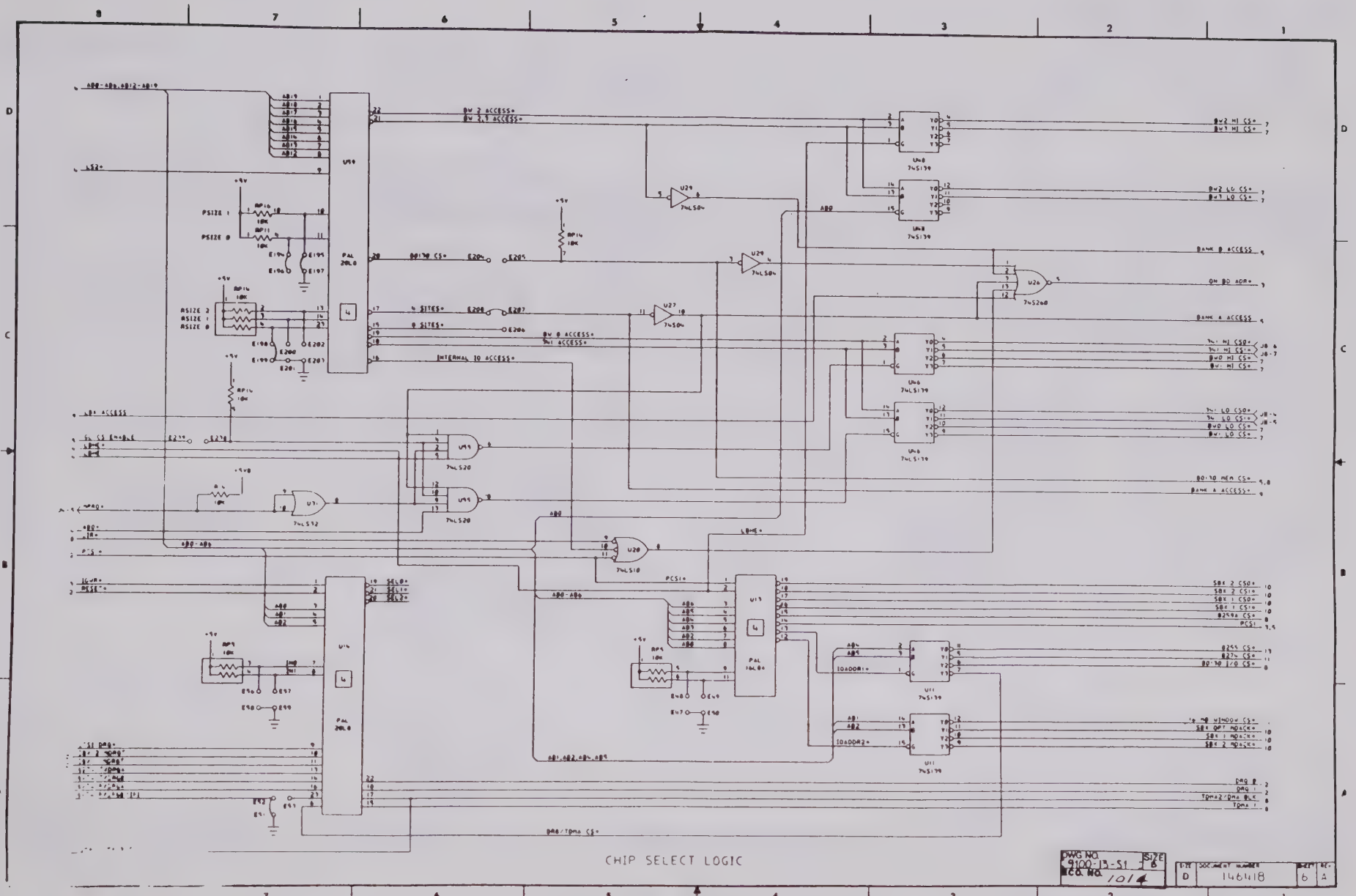

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Figure 5-2. Schematic Diagram (Sheet 6 of 13)

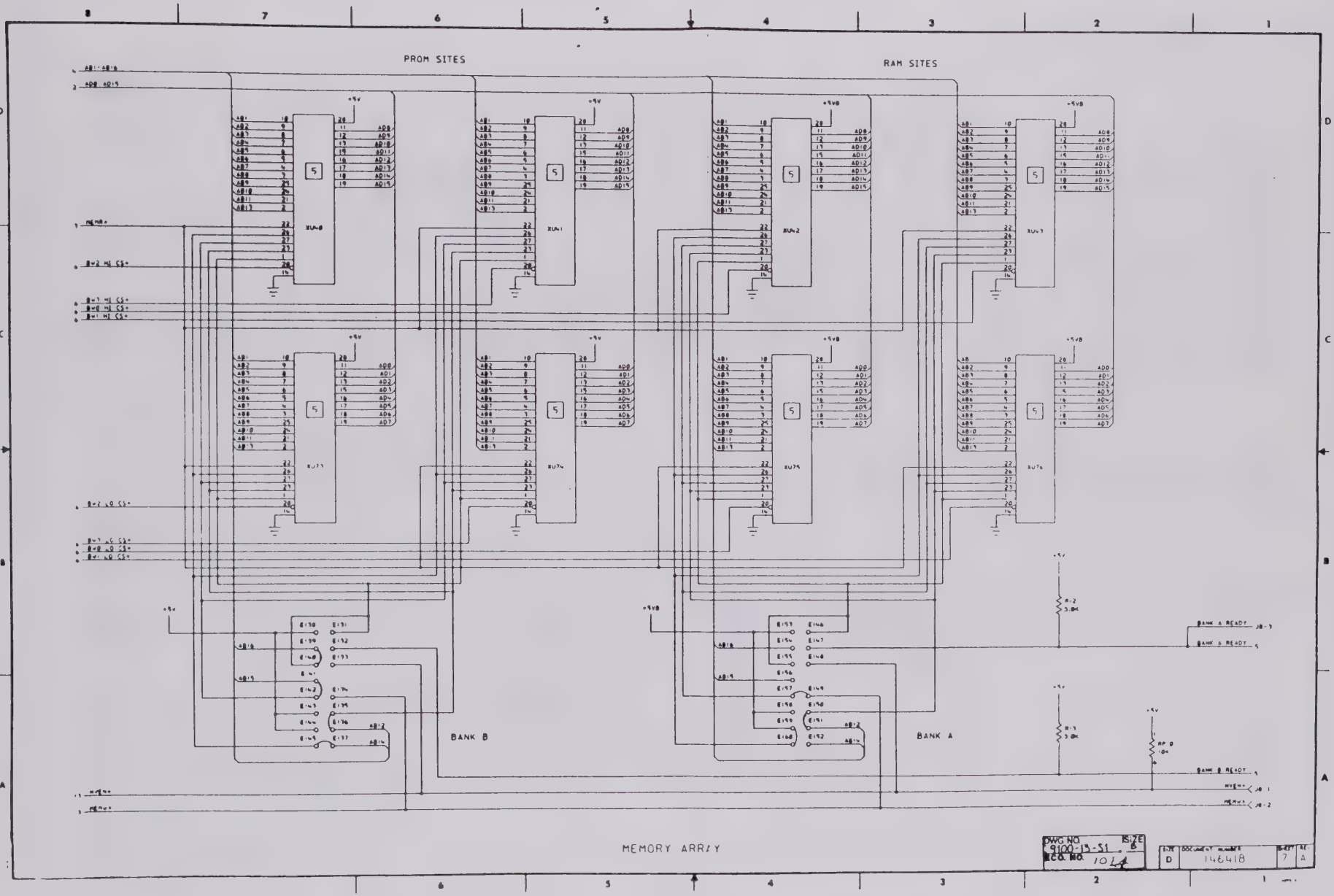

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Figure 5-2. Schematic Diagram (Sheet 7 of 13)

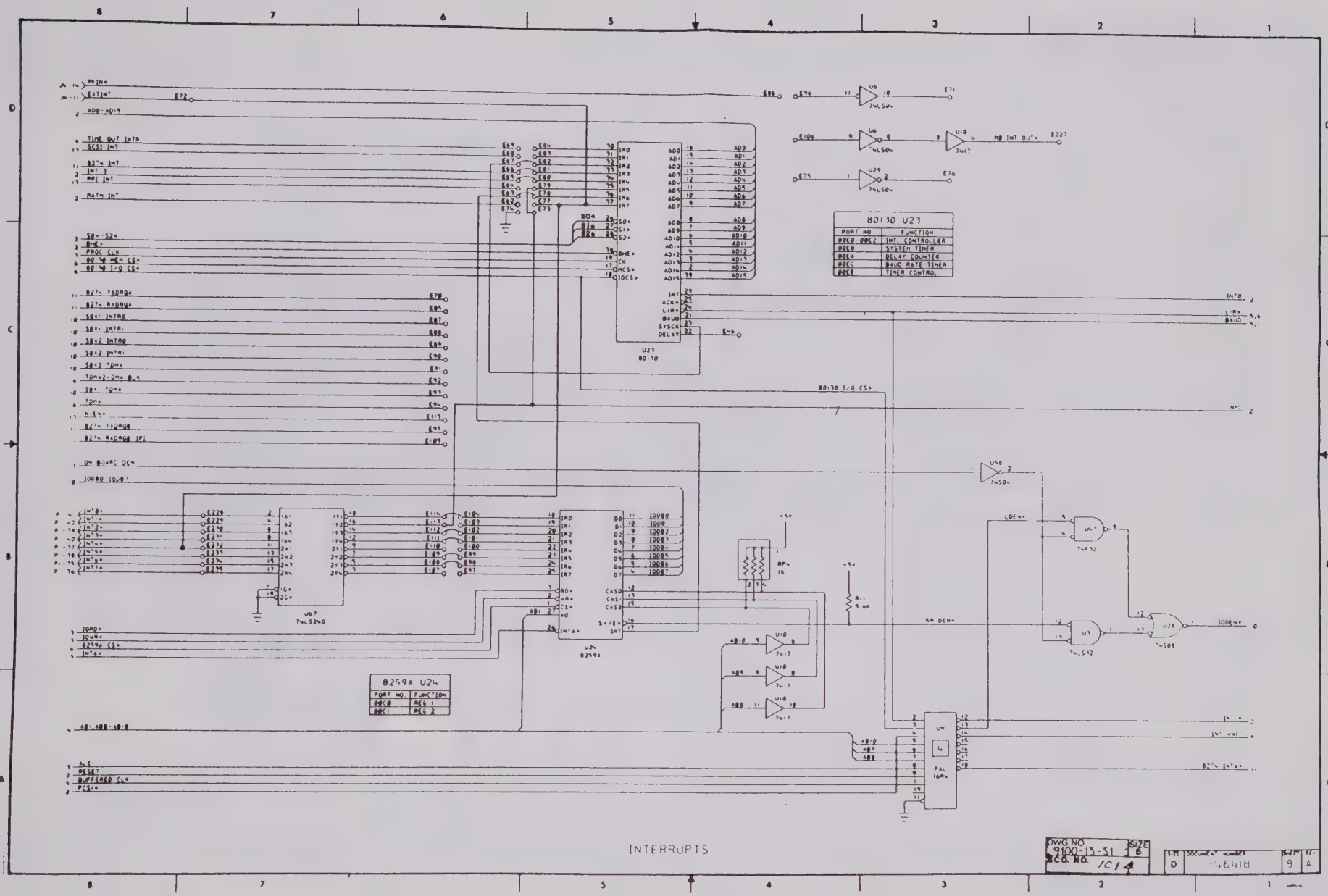

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Figure 5-2. Schematic Diagram (Sheet 8 of 13)

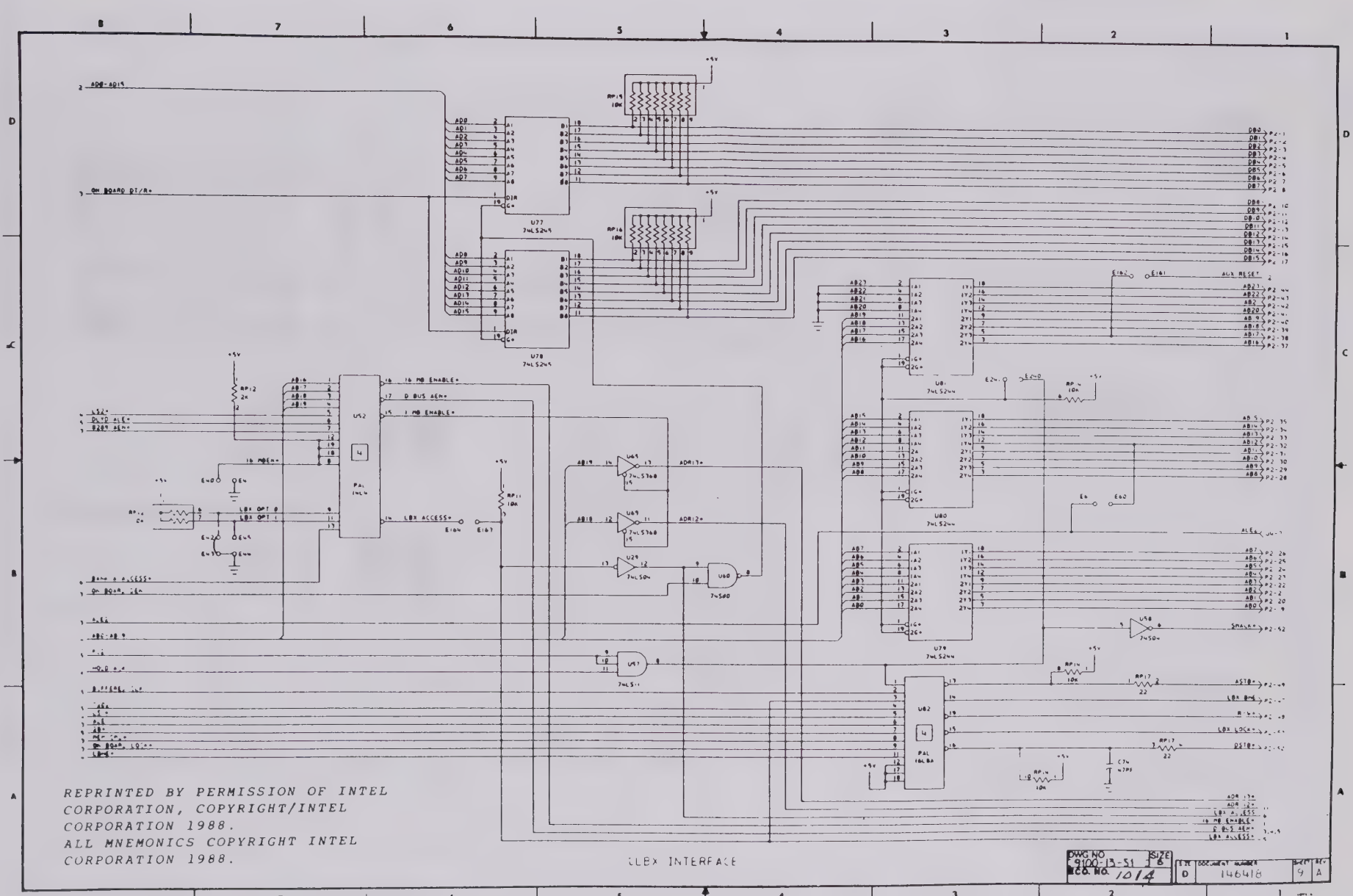

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Figure 5-2. Schematic Diagram (Sheet 9 of 13)

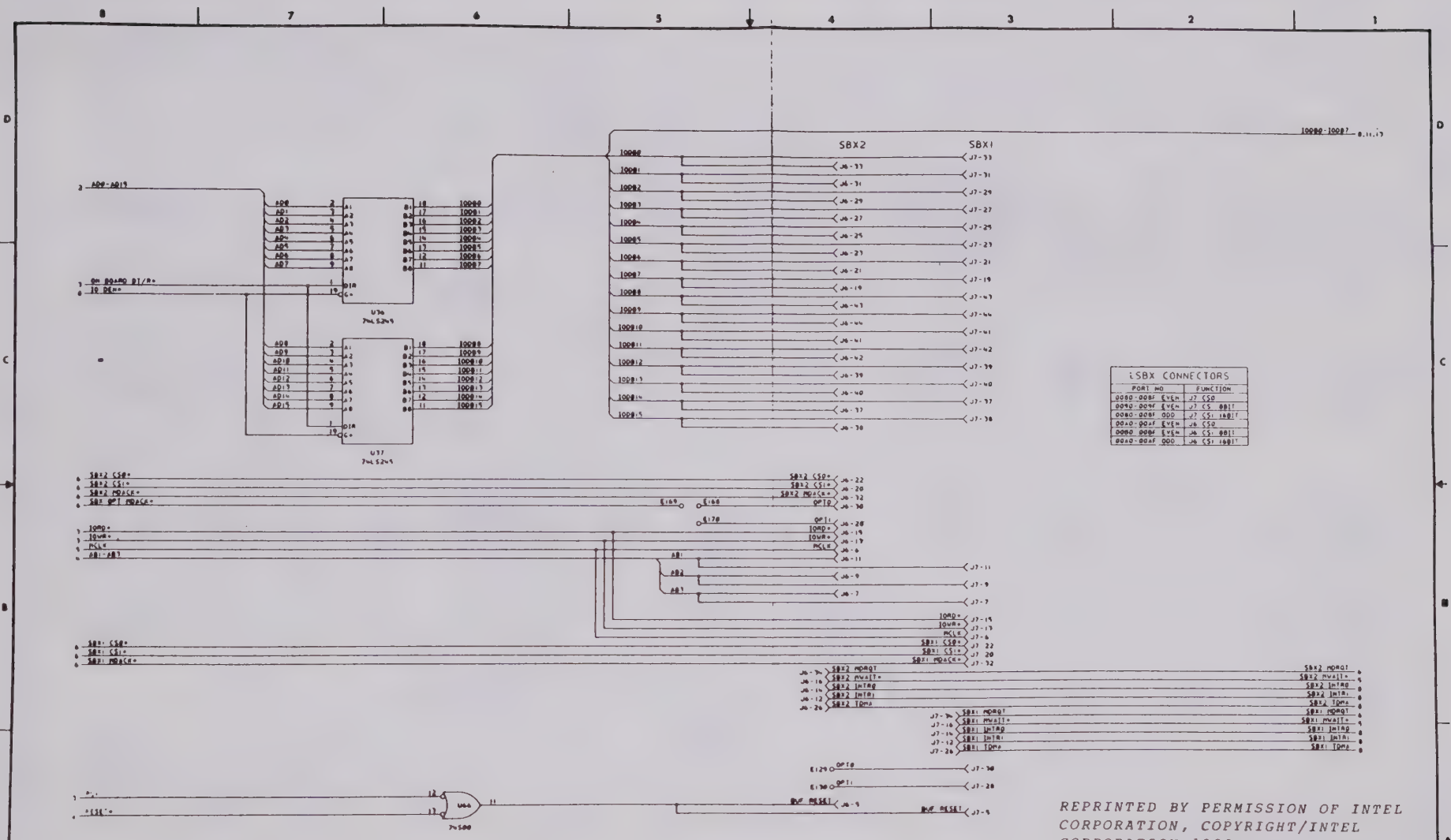

Figure 5-2. Schematic Diagram (Shee[illegible] 13)

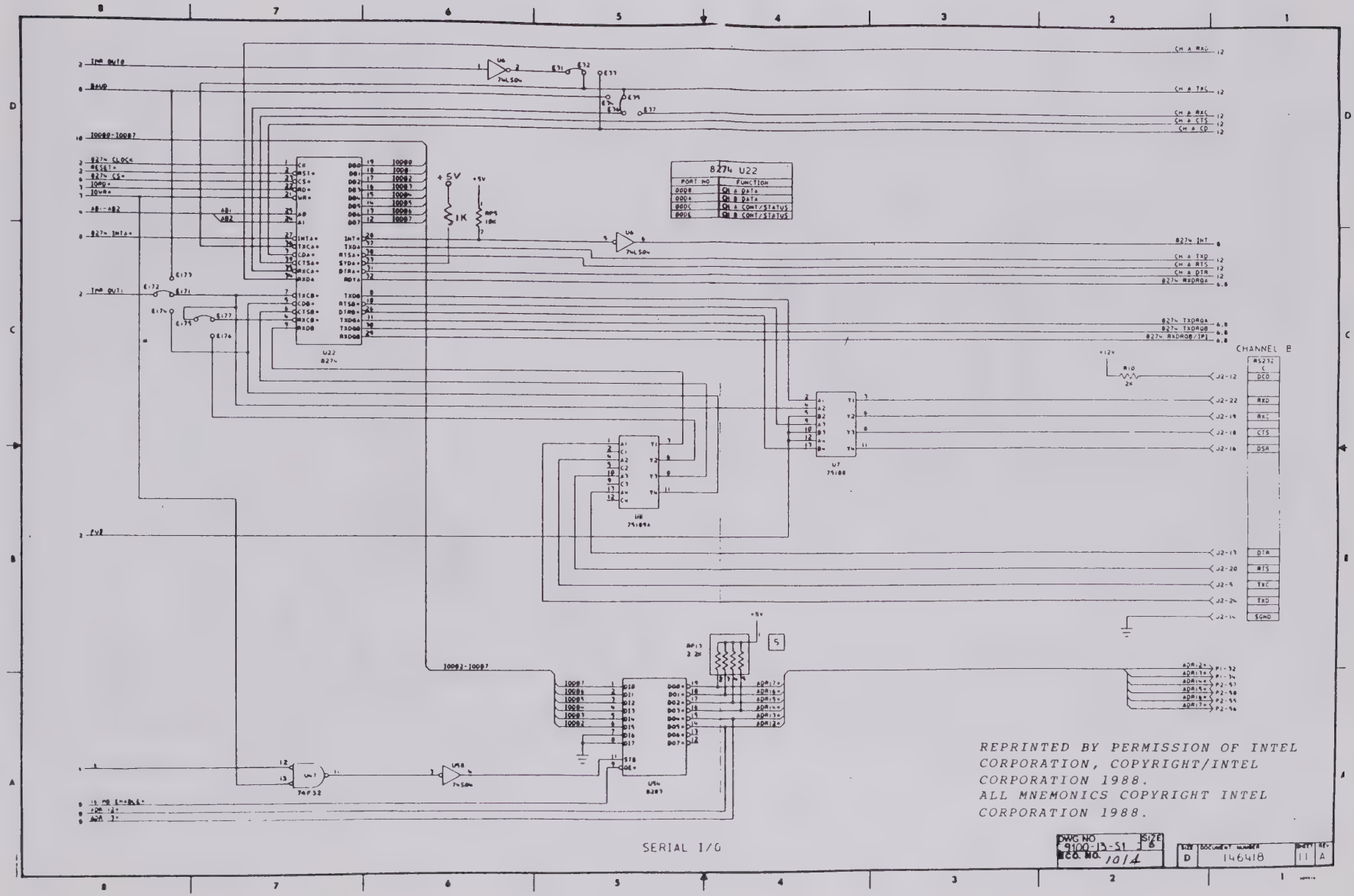

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Figure 5-2. Schematic Diagram (Sheet 11 of 13)

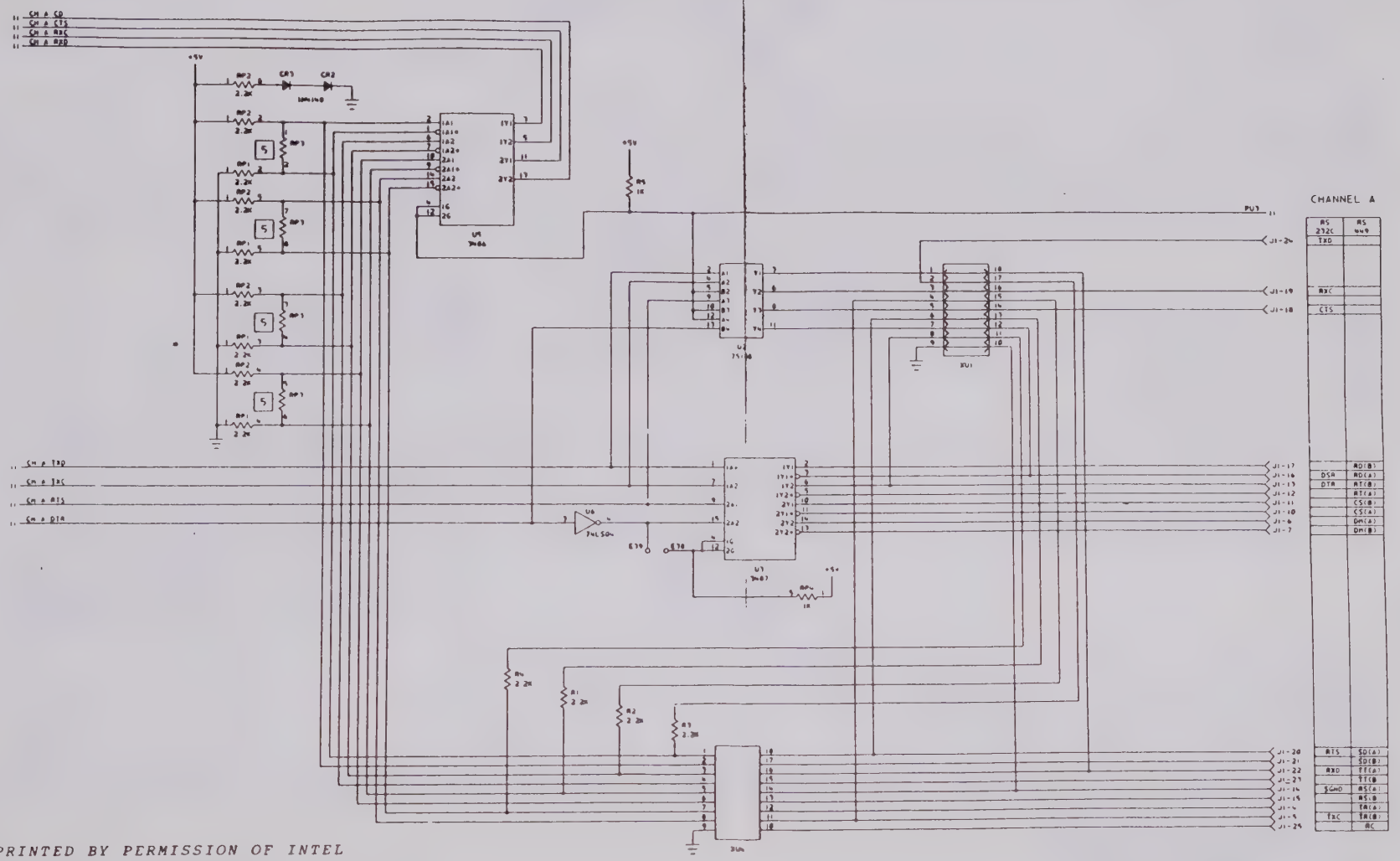

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Figure 5-2. Schematic Diagram (Sheet 1 of 13)

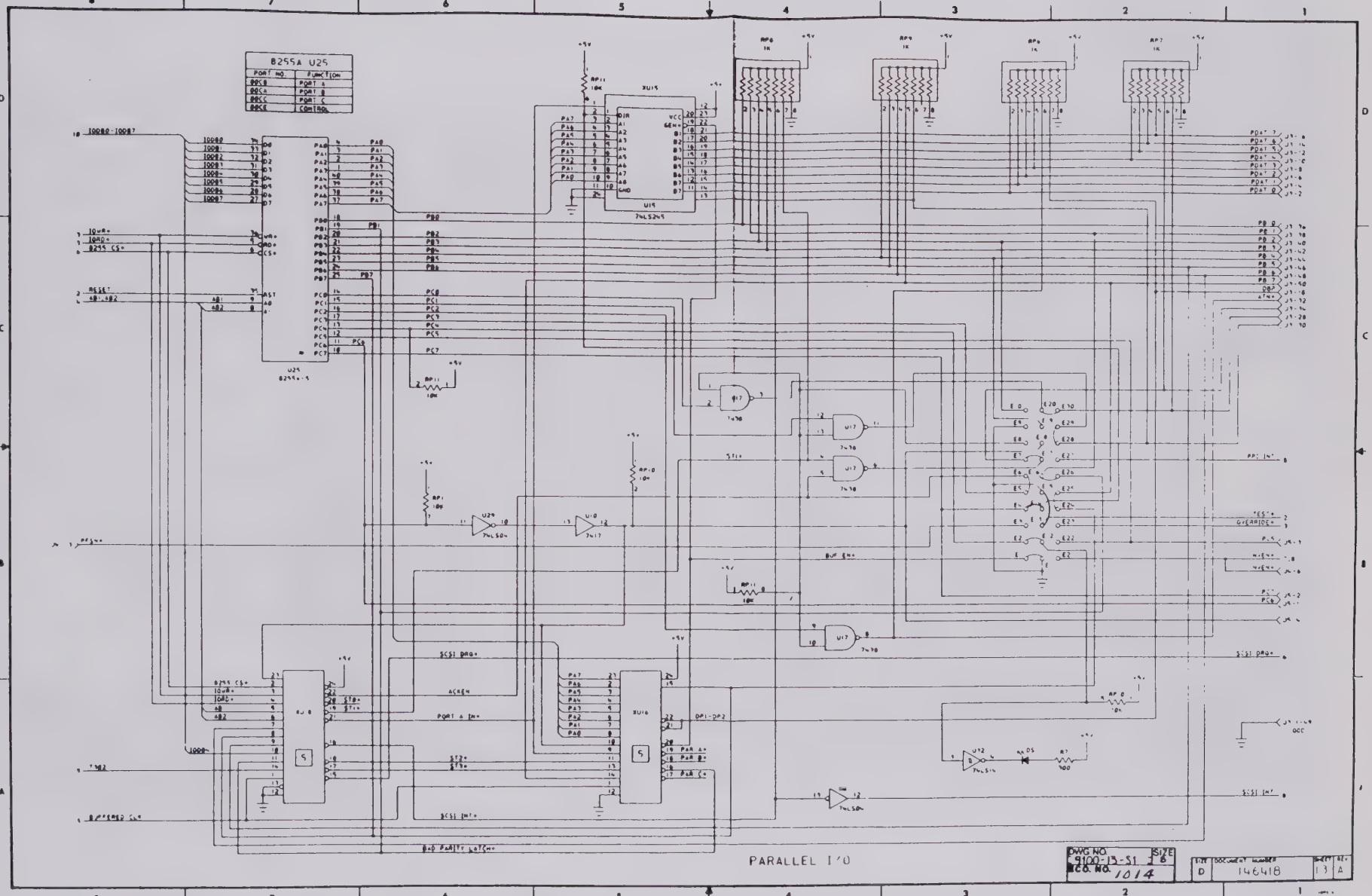

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Figure 5-2. Schematic Diagram (Sheet 13 of 13)

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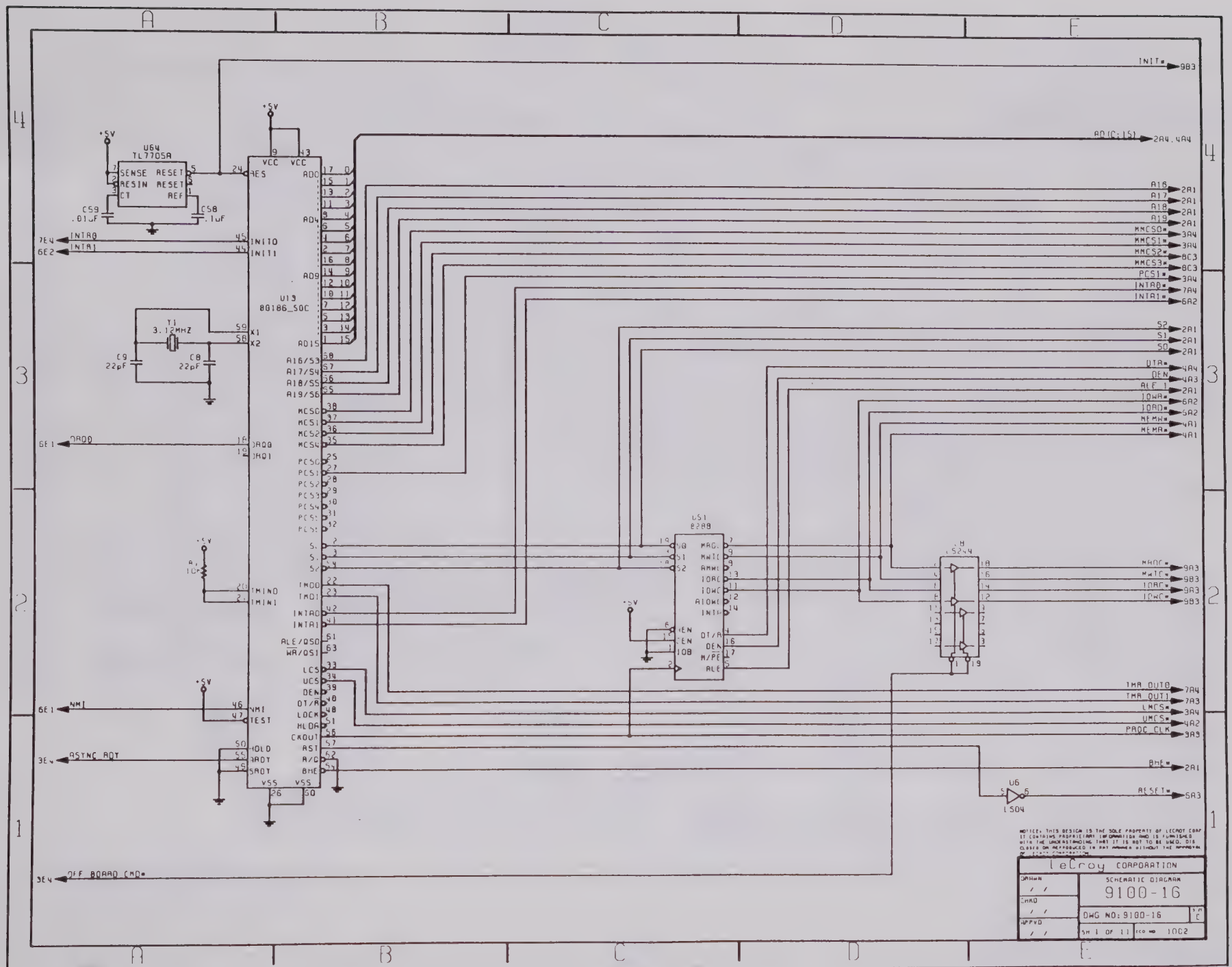
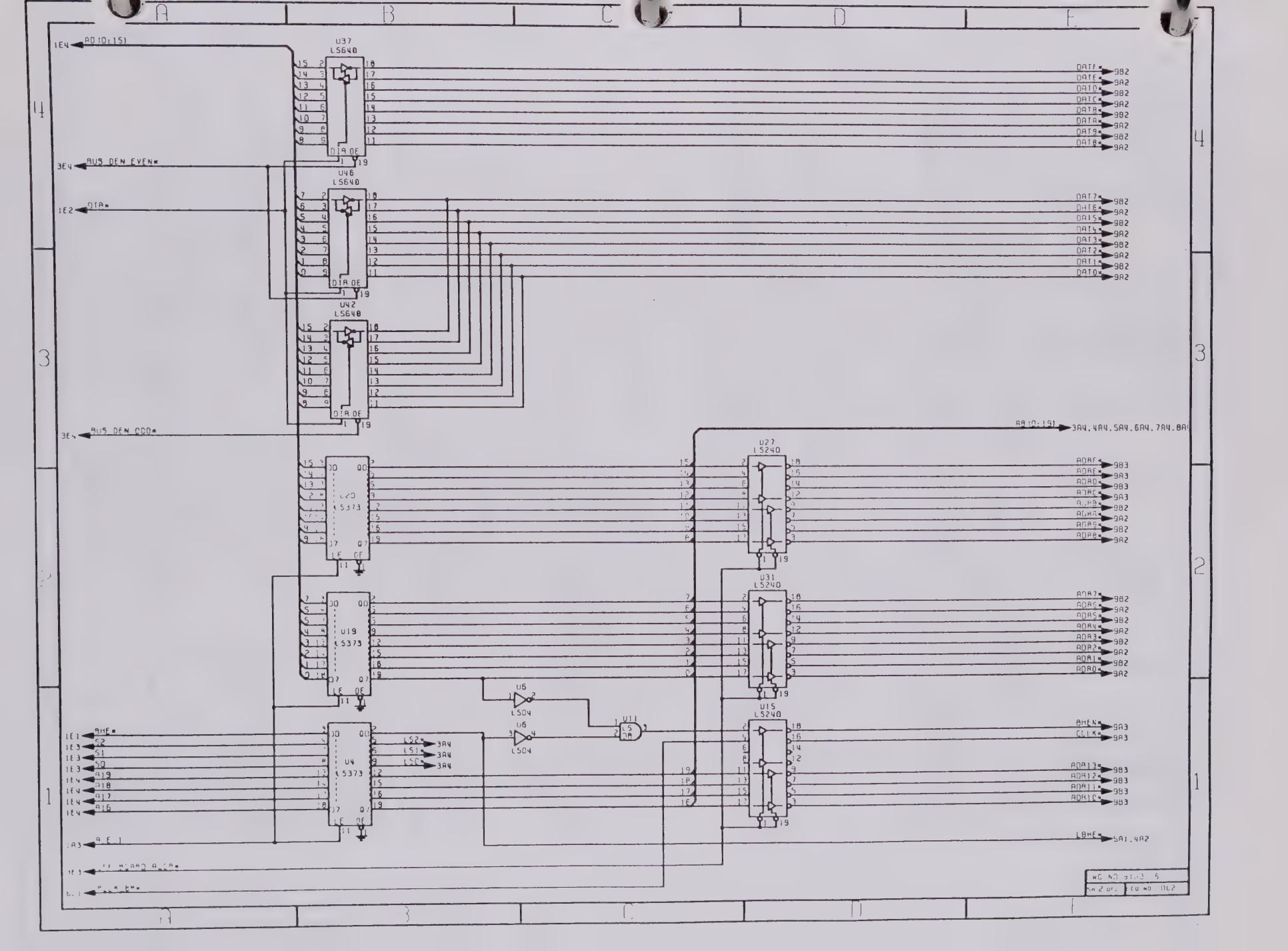
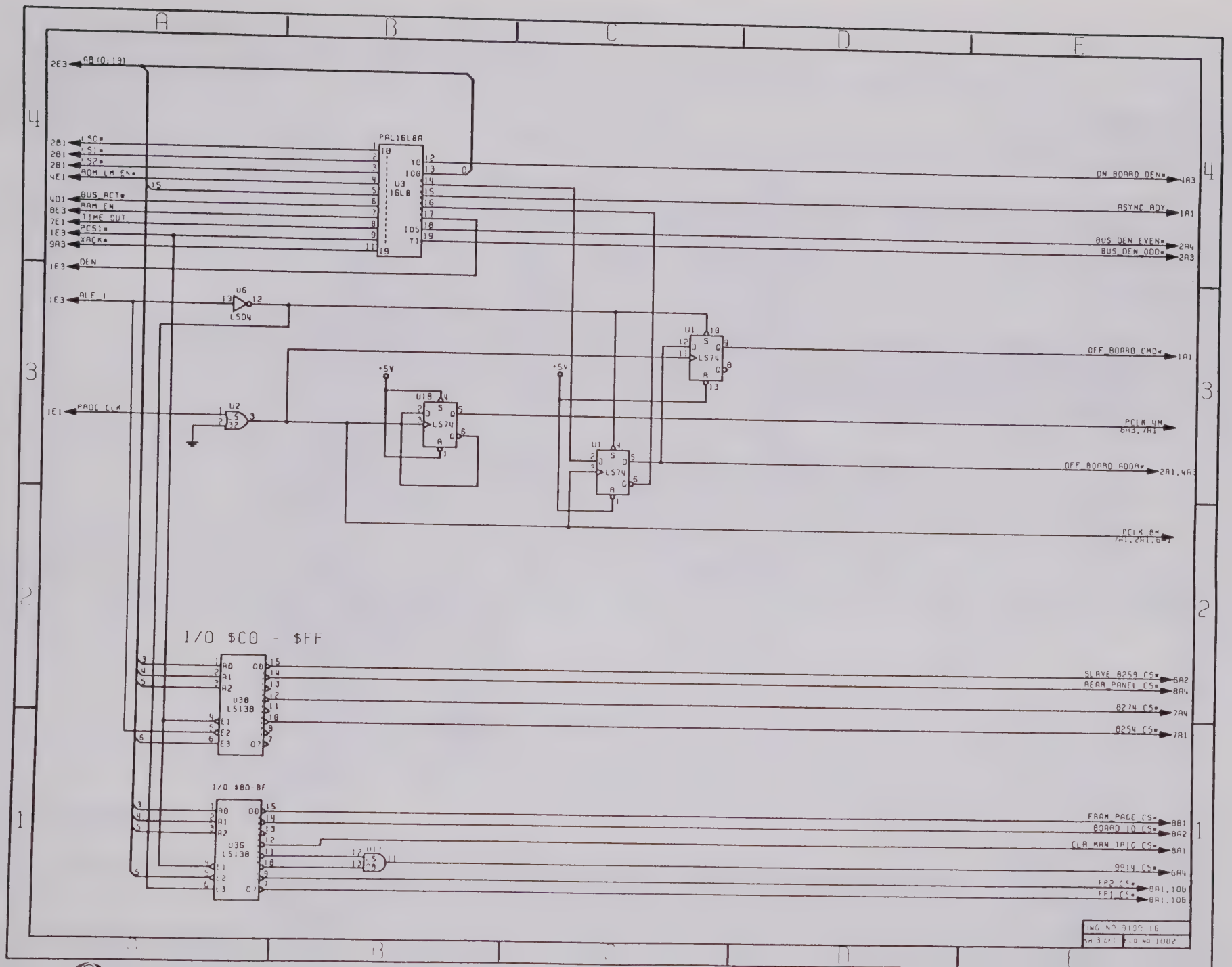
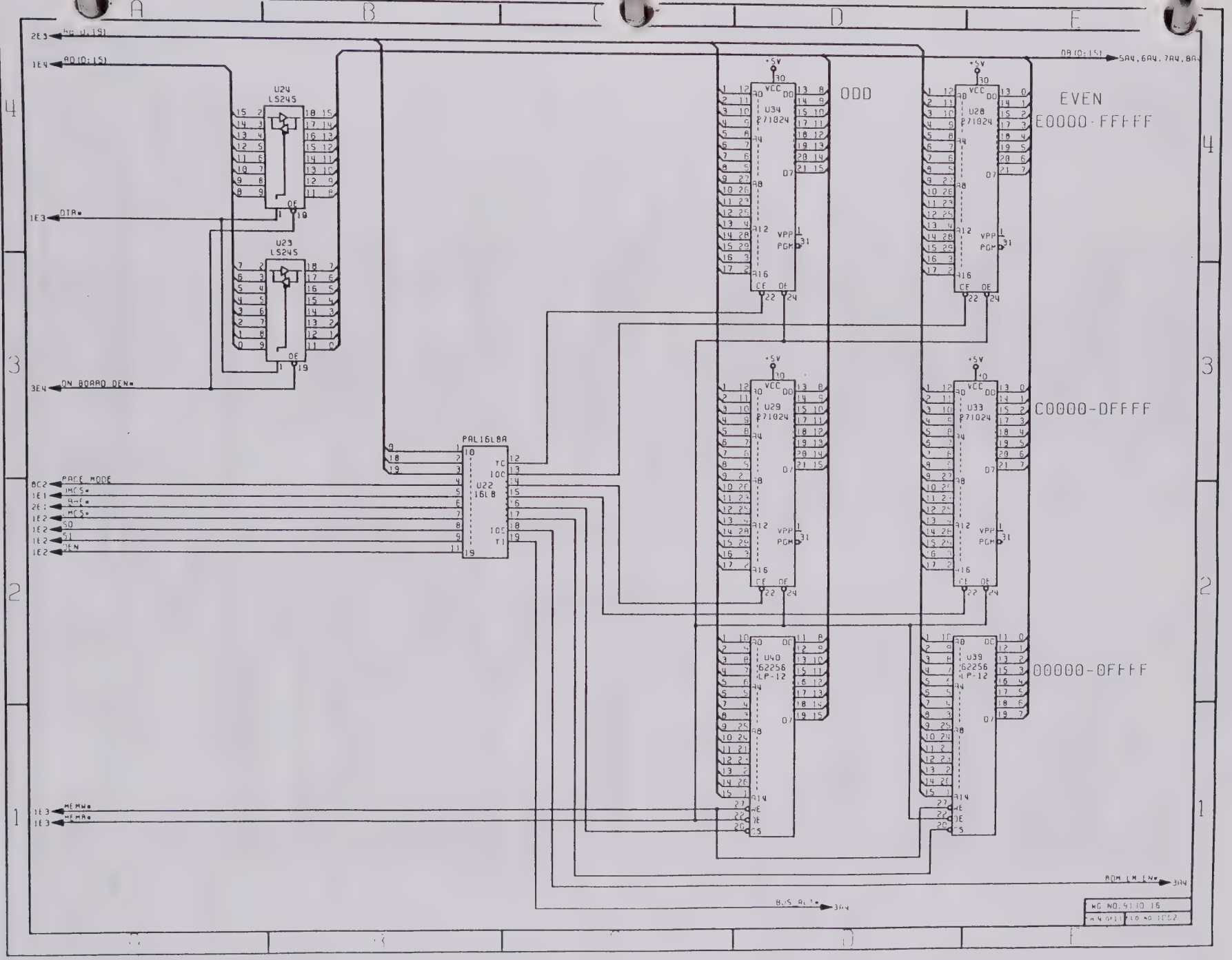
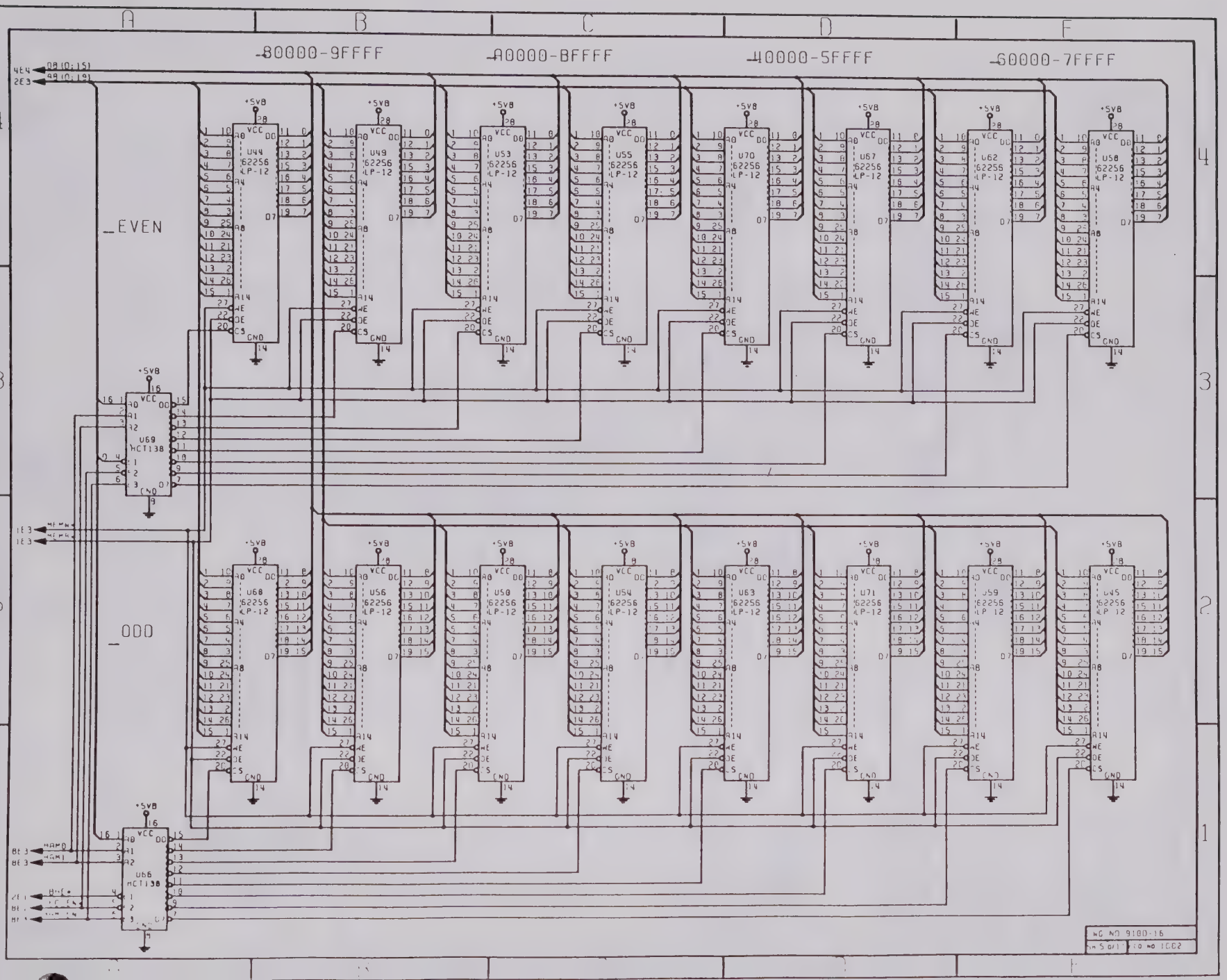
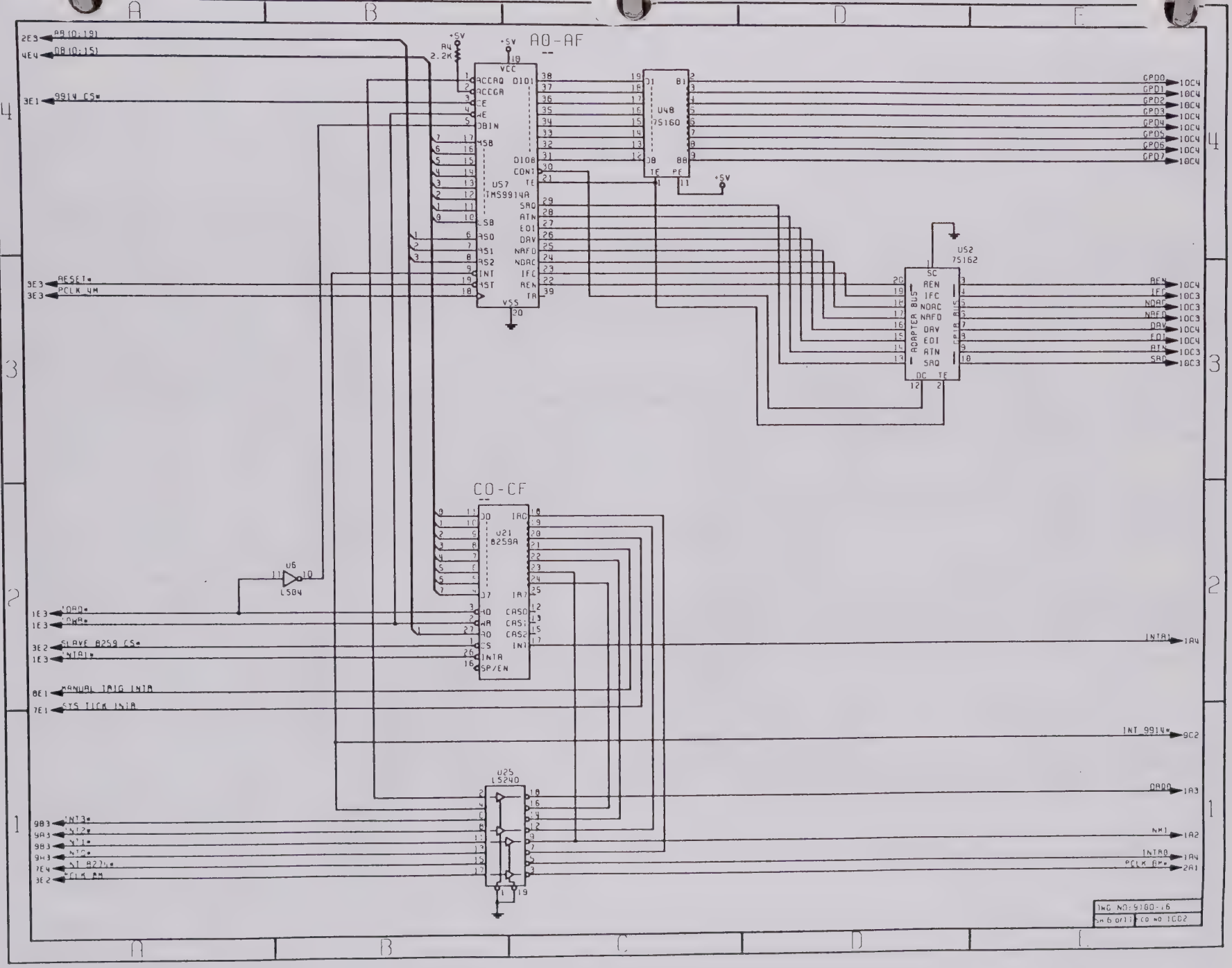

INIT*
AD[0:15]
A16
A17
A18
A19
MMCS0*
MMCS1*
MMCS2*
MMCS3*
PCS1*
INTA0*
INTA1*
S2
S1
S0
DTR*
DEN
ALE_1
IOWR*
IORD*
MEMW*
MEMR*
U64
TL7705A
SENSE RESET
RESIN RESET
CT REF
C59 .01uF
C58 .1uF
U13
80186_SOC
Y1
3.12MHZ
C9 22pF
C8 22pF
U51
8288
U6
LS04
TMR_OUT0
TMR_OUT1
LMCS*
UMCS*
PROC_CLK
BHE*
RESET*
NMI
ASYNC_RDY
OFF_BOARD_CMD*
LeCroy CORPORATION
SCHEMATIC DIAGRAM
9100-16
DWG NO: 9100-16

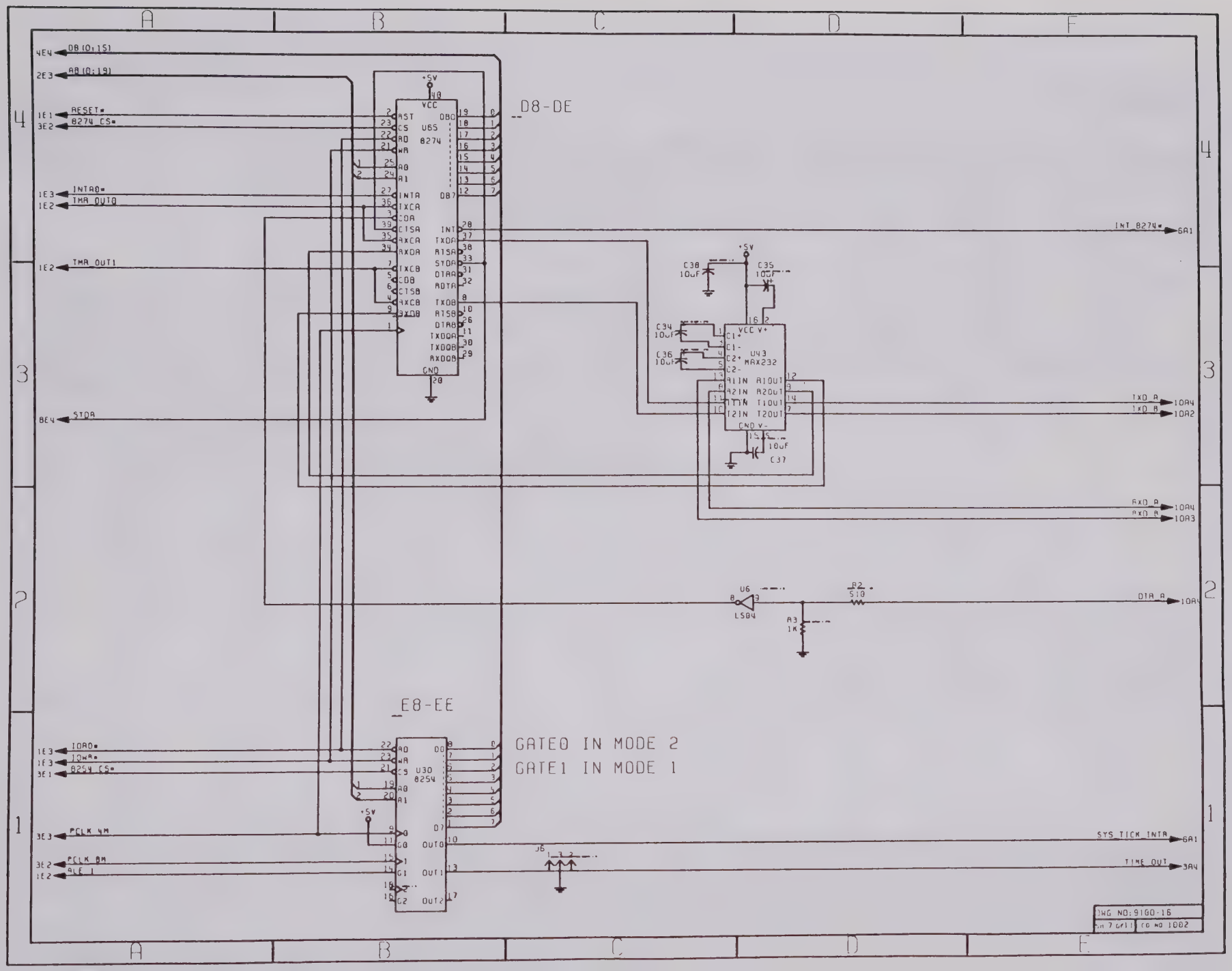

U37
LS640
U46
LS640
U42
LS640
BUS DEN EVEN*
BUS DEN ODD*
DIR*
AD[0:15]
U27
LS240
U31
LS240
U15
LS240
U20
LS373
U19
LS373
U4
LS373
U6
LS04
U11
LS
DIR OE

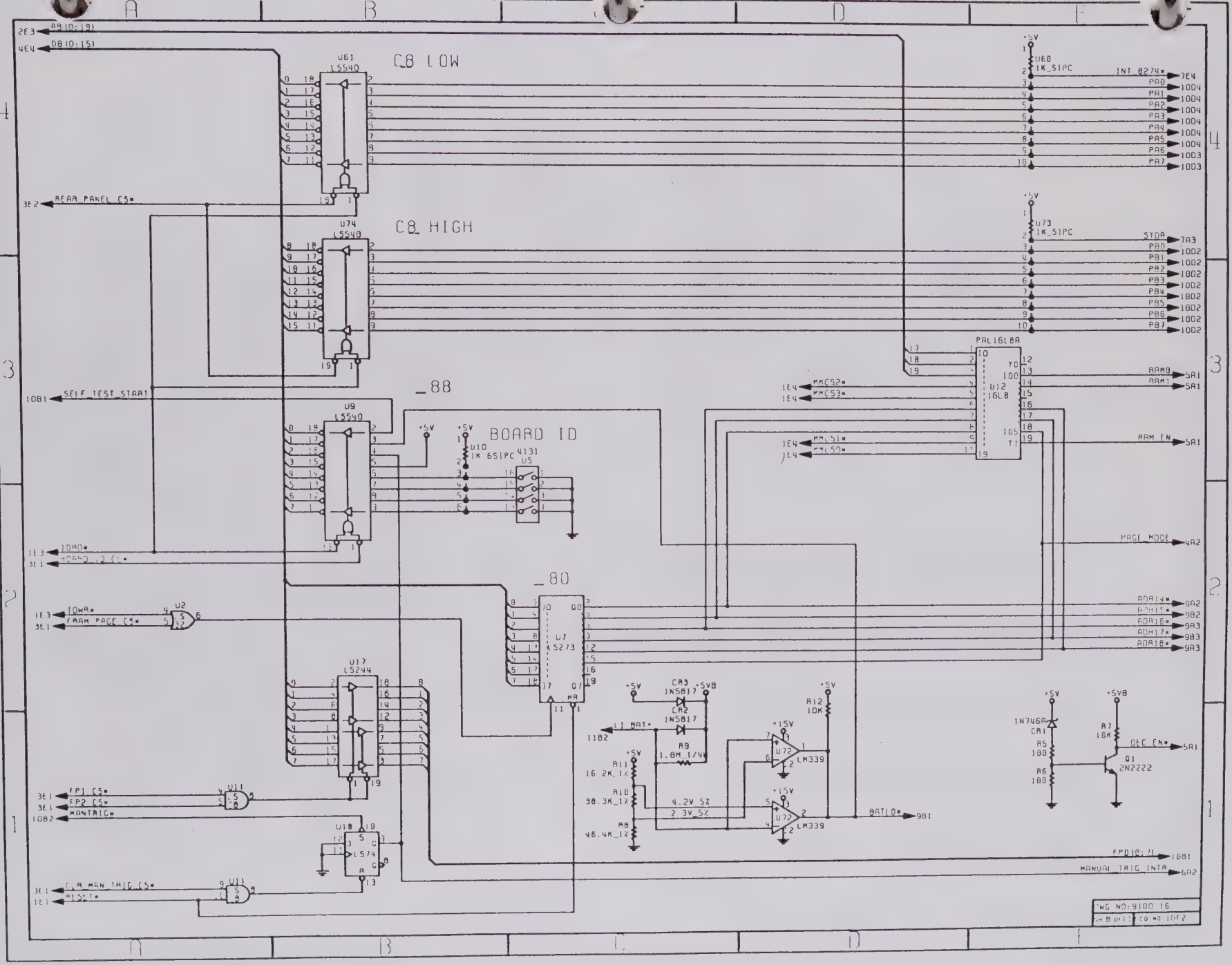

PAL16L8A
U3
16L8
LS04
LS74
LS138
I/O $C0 - $FF
I/O $80-BF
ON BOARD DEN*
ASYNC ADV
BUS DEN EVEN*
BUS DEN ODD*
OFF BOARD CMD*
PCLK 4M
OFF BOARD ADDR*
PCLK 8M
SLAVE 8259 CS*
AFAR PANEL CS*
8274 CS*
8254 CS*
FRAM PAGE CS*
BOARD ID CS*
CLR MAN TRIG CS*
9914 CS*
FP2 CS*
FP1 CS*

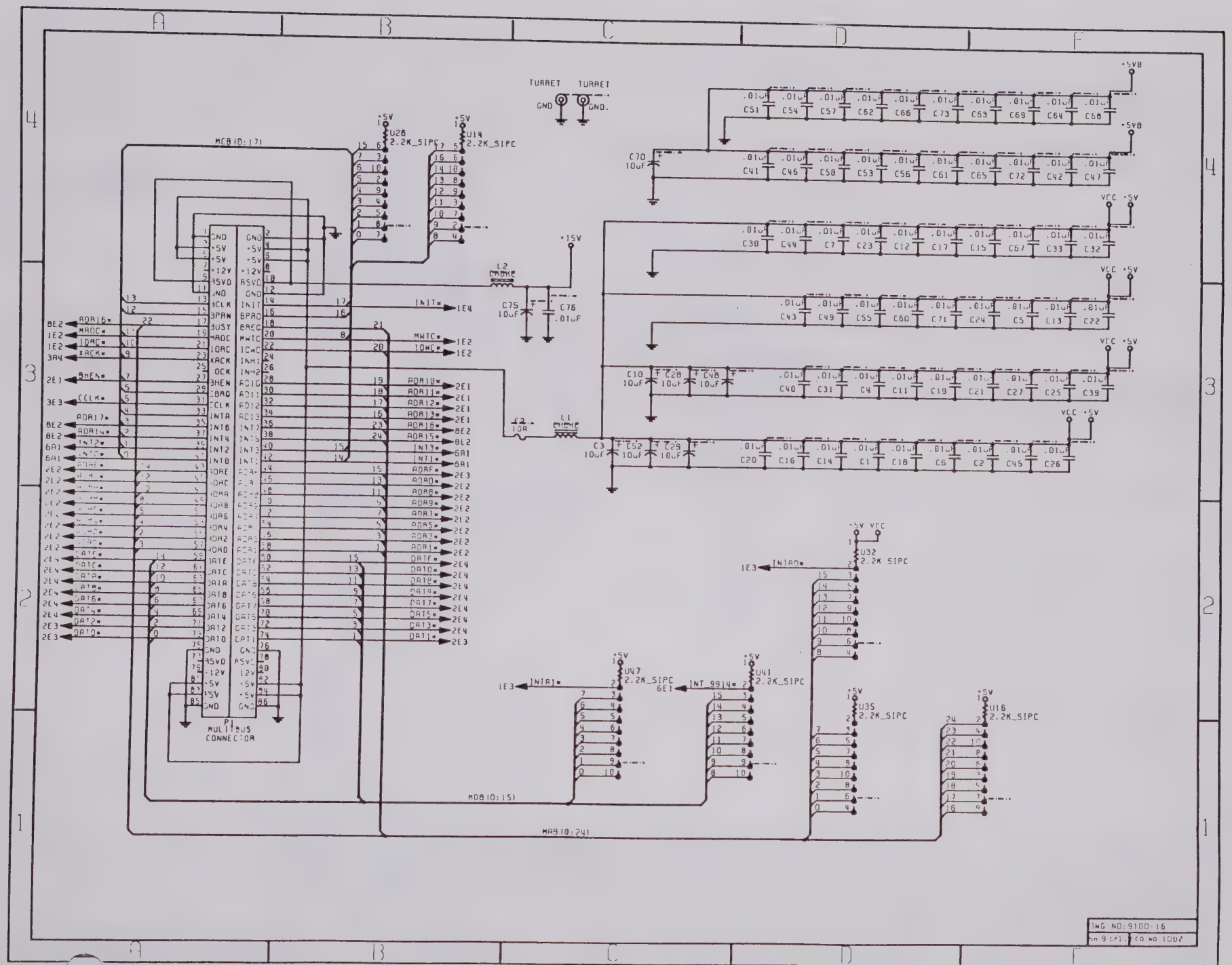

ODD
EVEN
E0000-FFFFF
C0000-DFFFF
00000-0FFFF
U24
LS245
U23
LS245
U34
U28
U29
U33
U40
U39
PAL16L8A
U22
16L8
PAGE MODE
ON BOARD DEN
DIR
MEMW
MEMR
BUS AL
ROM LM EN
SA4, 6A4, 7A4, 8A
AD10:15
DA10:15

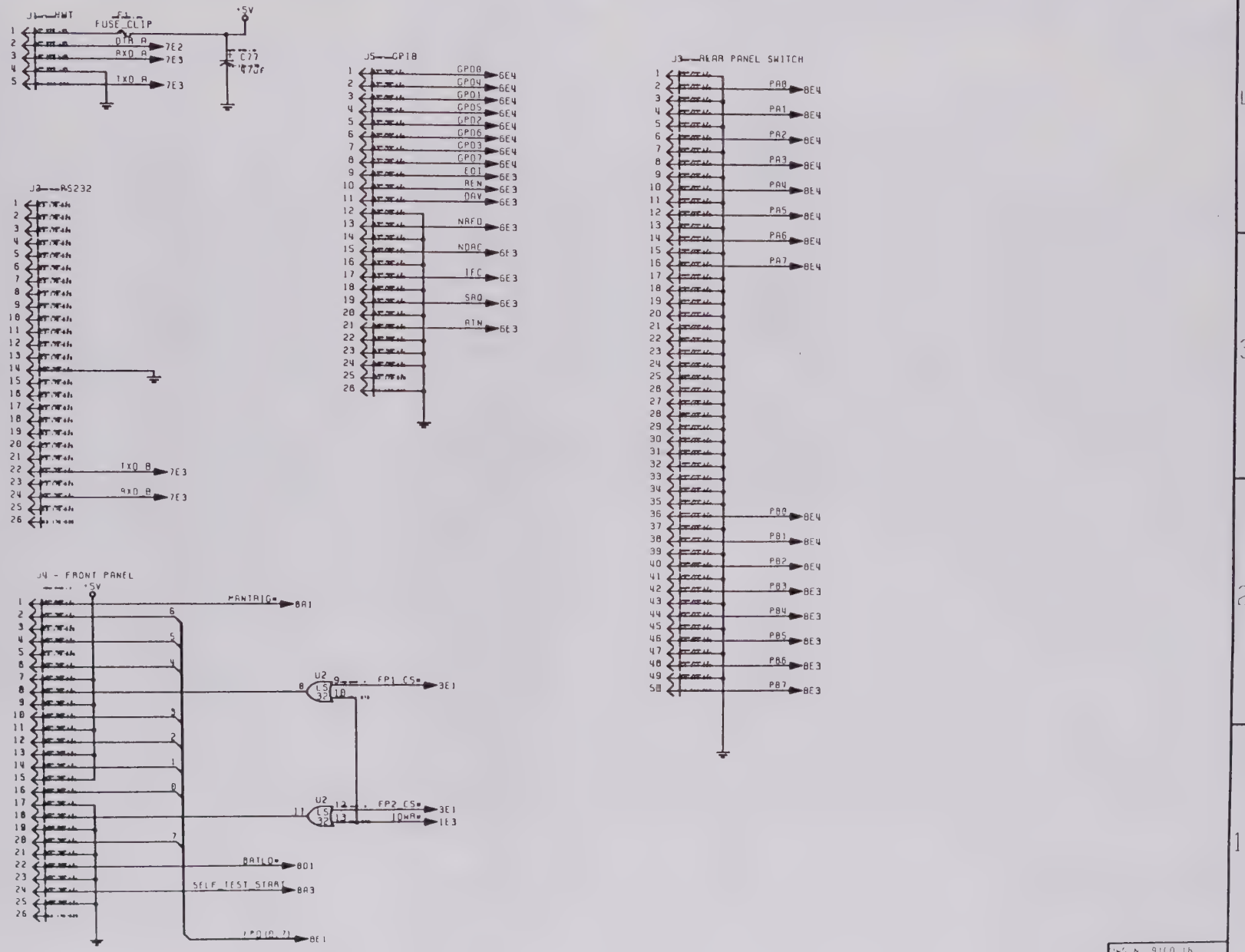

A
B
C
D
F
-80000-9FFFF
-A0000-BFFFF
-40000-5FFFF
-60000-7FFFF
_EVEN
_ODD
+5V8
U44
U49
U53
U55
U70
U67
U62
U58
U68
U56
U50
U54
U63
U71
U59
U65
U69
U66
74HCT138
62256
LP-12

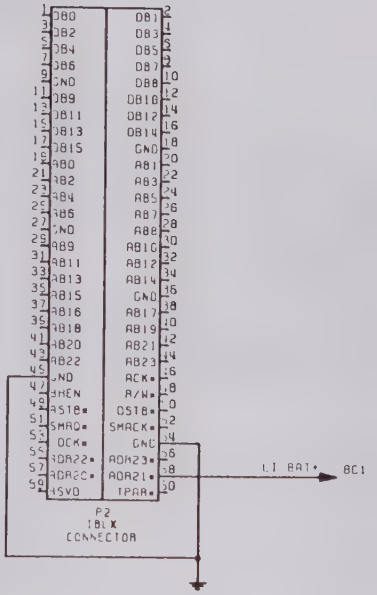

A0-AF
C0-CF
U57 TMS9914A
U48 75160
U52 75162
U21 8259A
U25 LS240
U6 LS04
ADAPTER BUS
GPD0
GPD1
GPD2
GPD3
GPD4
GPD5
GPD6
GPD7
REN
IFC
NDAC
NRFD
DAV
EOI
ATN
SRQ
INT 9914*
INTA1
INTA0
NM1
PCLK 8M*
9914 CS*
RESET*
PCLK 4M
SLAVE 8259 CS*
MANUAL TRIG INTA
SYS TICK INTA

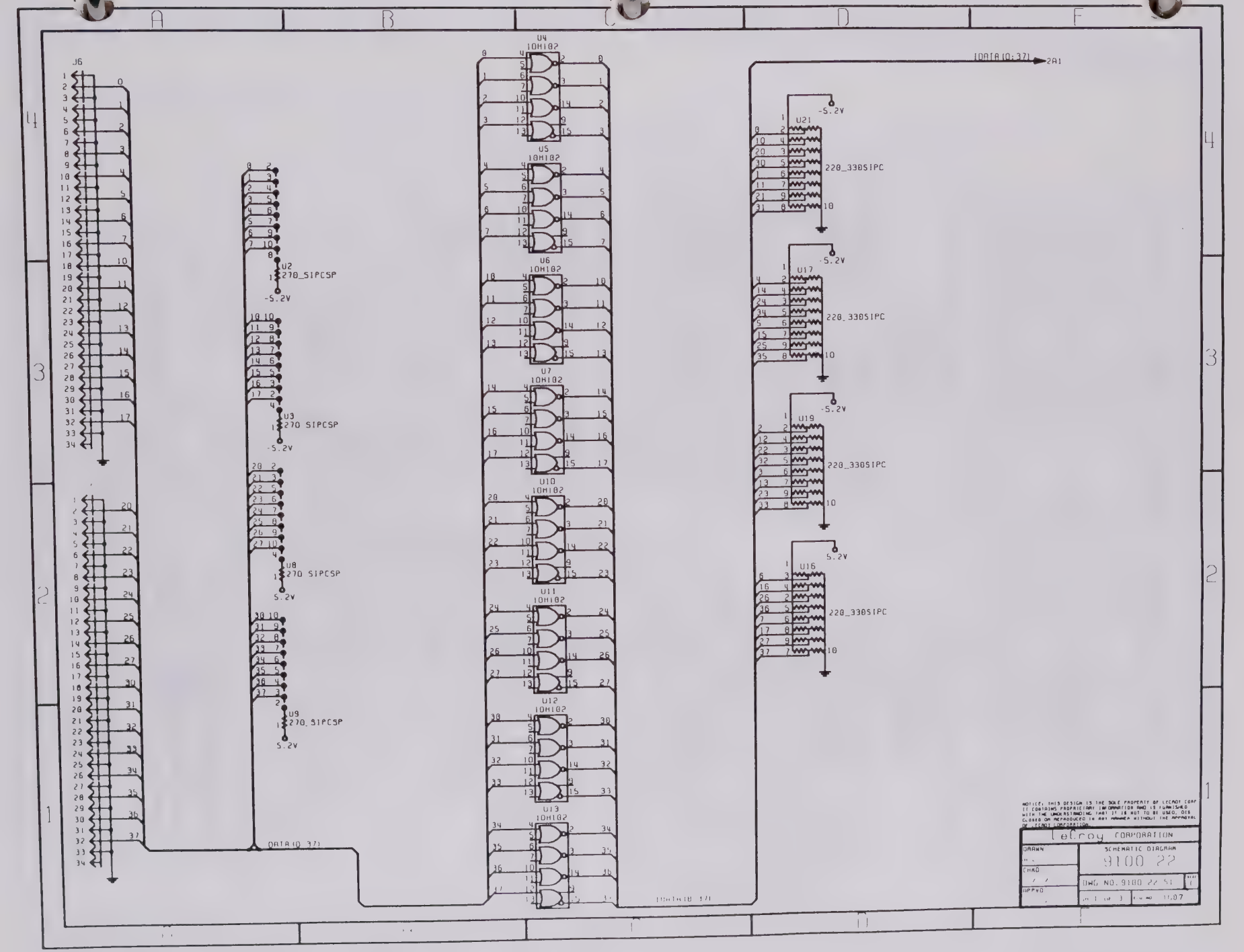

D8-DE
E8-EE
U65 8274
U30 8254
U43 MAX232
U6 LS04
GATE0 IN MODE 2
GATE1 IN MODE 1
DB(0:15)
AB(0:19)
RESET*
8274 CS*
INTA0*
TMR OUT0
TMR OUT1
STDA
IOAD*
IOWR*
8254 CS*
PCLK 4M
PCLK 8M
ALE 1
INT 8274*
TXD A
RXD A
DTR A
SYS TICK INTR
TIME OUT
DWG NO: 9160-16


C8 LOW
C8 HIGH
_88
_80
BOARD ID
U61
LS540
U74
LS540
U9
LS540
U10
1K 6S1PC
U5
4131
U60
1K_SIPC
U73
1K_SIPC
U12
16L8
PAL16L8A
U7
LS273
U17
LS244
U18
LS74
U2
U11
U72
LM339
U72
LM339
CR3
1N5817
CR2
1N5817
CR1
1N746A
A9
1.8M_1/4W
A11
16.2K_1Z
A10
30.3K_1Z
A8
46.4K_1Z
A12
10K
A7
10K
A5
100
A6
100
Q1
2N2222
4.2V 5%
2.3V 5%
REAR PANEL CS*
SELF_TEST_START
IOWR*
FRAM PAGE CS*
FP1 CS*
FP2 CS*
MANTRIG*
C_A_MAN_TRIG_CS*
RESET*
INT 8274*
STDA
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
MMCS2*
MMCS3*
MM_S1*
MM_S0*
RAM_EN
PAGE_MODE
BATLO*
DEC_EN*
FPD[8:1]
MANUAL_TRIG_INTR
DWG NO: 9100 16
SHEET NO: 1OF2


TURRET
TURRET
GND
GND
+5V
+15V
+5VB
VCC
U28
2.2K_SIPC
U14
2.2K_SIPC
U32
2.2K SIPC
U47
2.2K_SIPC
U41
2.2K_SIPC
U35
2.2K_SIPC
U16
2.2K_SIPC
L2
CHOKE
L1
CHOKE
F2
10A
C75
10uF
C76
.01uF
C70
10uF
C10
10uF
C28
10uF
C48
10uF
C3
10uF
C52
10uF
C29
10uF
.01uF
MCB[0:17]
MDB[0:15]
MAB[0:24]
INIT*
MWTC*
IOWC*
INTA0*
INTA1*
INT_9914*
P1
MULTIBUS
CONNECTOR
DWG NO: 9100-16


J1 — AUT
FUSE_CLIP
+5V
C77
TXD_A
RXD_A
TXD_A
J2 — RS232
TXD_B
RXD_B
J5 — GPIB
GPD0
GPD4
GPD1
GPD5
GPD2
GPD6
GPD3
GPD7
EOI
REN
DAV
NRFD
NDAC
IFC
SRQ
ATN
J3 — REAR PANEL SWITCH
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
J4 - FRONT PANEL
+5V
MAINTIC=
U2
FP1_CS=
FP2_CS=
IOWR=
BATLO=
SELF_TEST_STAR


DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
GND
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
GND
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
GND
AB8
AB9
AB10
AB11
AB12
AB13
AB14
AB15
GND
AB16
AB17
AB18
AB19
AB20
AB21
AB22
AB23
GND
ACK*
WHEN
R/W*
AS1B*
DS1B*
SMRQ*
SMACK*
OCK*
GND
ADA22*
ADA23*
ADA21*
ADA20*
+5VD
TPAA*
LI BAT*
BC1
P2
IBLX
CONNECTOR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U2
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-5.2V
U3
270 SIPCSP
-5.2V
U8
270 SIPCSP
5.2V
U9
270_SIPCSP
5.2V
DATA(0:37)
U4
10H102
U5
10H102
U6
10H102
U7
10H102
U10
10H102
U11
10H102
U12
10H102
U13
10H102
DATA(0:37)
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U21
-5.2V
220_330SIPC
U17
-5.2V
220_330SIPC
U19
-5.2V
220_330SIPC
U16
5.2V
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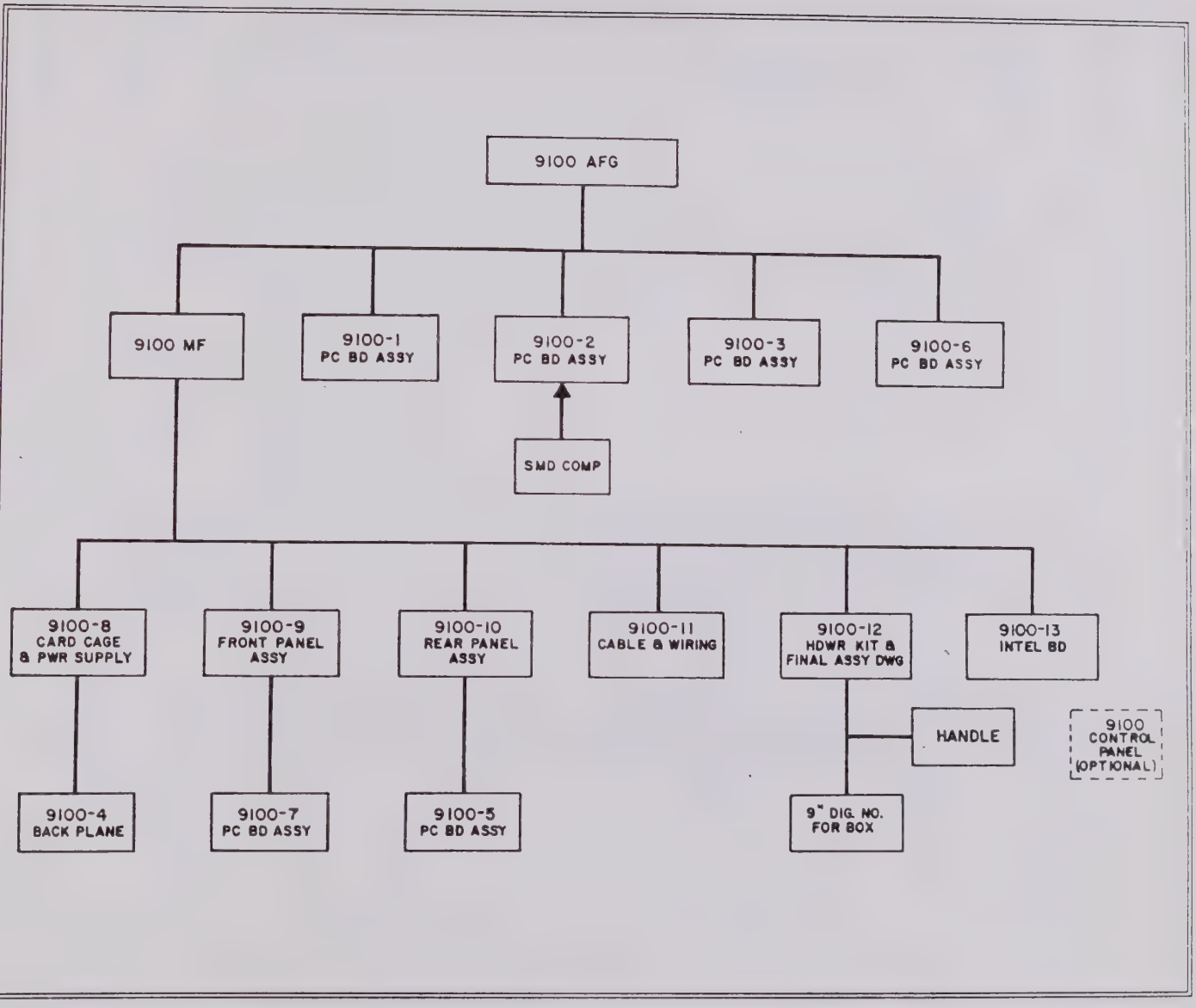
ecroy CORPORATION
SCHEMATIC DIAGRAM
9100 22
DRAWN
CHAD
APPVD
DWG. NO. 9100 22 SI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9100 MF
9100-1
PC BD ASSY
9100-2
PC BD ASSY
9100-3
PC BD ASSY
9100-6
PC BD ASSY
SMD COMP
9100-8
CARD CAGE
& PWR SUPPLY
9100-9
FRONT PANEL
ASSY
9100-10
REAR PANEL
ASSY
9100-11
CABLE & WIRING
9100-12
HDWR KIT &
FINAL ASSY DWG
9100-13
INTEL BD
HANDLE
9100
CONTROL
PANEL
(OPTIONAL)
9100-4
BACK PLANE
9100-7
PC BD ASSY
9100-5
PC BD ASSY
9" DIG. NO.
FOR BOX

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100 ARBITRARY FUNC GEN UM: EA PC: 4 ECN: 1000 ASSEMBLY QTY: 1
ERC: AA SRCE CODE: G TYPE: 1 ABC: A PL: F DATE: 22-Aug-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0008	205271064		IC 8K X 8 RAM 7164S									
		4	IC	P 1 A P EA	8	22-Aug-90		31-Dec-99		100	0	PROD
0010	9100-16	P	COMPLETED BOARD 9100-16									
		4	ASSY	A 1 P A P EA	1	10-May-89		31-Dec-99		600	0	SSDSUB
0007	9100-18	E	HI SPEED MEMORY BD 9100-18									
		4	ASSY	A 1 D P EA	1	01-Aug-90		31-Dec-99		600	0	SSDSUB
0002	9100-2	R	ANALOG BD									
		4	ASSY	A 1 P A P EA	1	02-Jun-86		31-Dec-99		600	0	SSDSUB
0006	9100-6	BB	TIMEBASE BD									
		4	ASSY	A 1 P A P EA	1	02-Jun-86		31-Dec-99		600	0	SSDSUB
0012	9100-9	N	FRONT PNL ASS'Y 9100-9									
		4	ASSY	A 1 P B P EA	1	21-Feb-89		31-Dec-99		600	0	SSDSUB
0005	9100/OM	A	9100 OPERATOR MANUAL									
		4	ASSY	A 1 P C P EA	1	17-Jan-90		31-Dec-99		100	0	SSDSUB
0004	9100MF	G	MAIN FRAME ASS'Y 9100									
		4	ASSY	A 1 P A P EA	1	30-Jul-86		31-Dec-99		600	0	SSDSUB

NOTES:

END OF REPORT

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-1 HI SPEED MEMORY BD 9100-1 UM: EA PC: 4 ECN: 1011 ASSEMBLY QTY: 1
ERC: Z SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 13-Jun-89

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0051	103276103		CAP CERA MONO X7R .01 UF									
			CAP	P 1 B P EA	95	29-Dec-87		31-Dec-99		100	0	PROD
			C26-C37,C39-C121									
0001	103327103		CAP CERA MONO 50V .01 UF									
			CAP	P 1 A P EA	18	14-Jul-87		31-Dec-99		100	0	PROD
			C122-C139									
0109	142124476		CAP TANT DIP CASE 47 UF									
			CAP	P 1 B P EA	10	06-May-88		31-Dec-99		100	0	PROD
			C1-C10									
0103	146424106		CAP MINI ALUM 20% 10 UF									
			CAP	P 1 B P EA	15	29-Dec-87		31-Dec-99		100	0	PROD
			C11-C25									
0097	161225820		RES CARBON FILM 82 OHMS									
			RES	P 1 B P EA	1	08-Apr-87		31-Dec-99		100	0	PROD
			R2									
0091	161335131		RES CARBON FILM 130 OHMS									
			RES	P 1 B P EA	1	14-Jul-87		31-Dec-99		100	0	PROD
			R1									
0015	190842471		RESISTOR NETWORK 470 OHMS									
			RES	P 1 B P EA	5	02-Sep-86		31-Dec-99		100	0	PROD
			RP5,RP6,RP7,RP8,RP9									
0104	200031028		IC 2-INPUT NAND SN74LS00N									
			IC	P 1 B P EA	1	29-Dec-87		31-Dec-99		100	0	PROD
			U51									
0080	200031040		IC 3-INPUT NAND SN74S10N									
			IC	P 1 B P EA	1	14-Jan-87		31-Dec-99		100	0	PROD
			U39									
0089	200031044		IC 5-INPUT NOR SN74S260N									
			IC	P 1 B P EA	1	31-Mar-86		31-Dec-99		100	0	PROD
			U54									
0005	200031046		IC HEX INVERTER SN74LS04N									
			IC	P 1 B P EA	1	14-Jan-87		31-Dec-99		100	0	PROD
			U52									
0092	200031049		IC D-TYP FLOP SN74LS74N									
			IC	P 1 B P EA	3	29-Jun-88		31-Dec-99		100	0	PROD
			U1,U11,U12									
0093	200031073		IC 2-IN POS OR SN74LS32N									
			IC	P 1 B P EA	2	14-Jan-87		31-Dec-99		100	0	PROD
			U5,U27									
0009	200031077		IC 3-INPUT AND SN74LS11N									
			IC	P 1 B P EA	1	14-Jan-87		31-Dec-99		100	0	PROD
			U26									
0059	200031083		IC 2-INPUT POS OR SN74S32									
			IC	P 1 B P EA	2	14-Jan-87		31-Dec-99		100	0	PROD
			U30,U31									
0082	200031086		IC 2-INPUT AND SN74LS08N									
			IC	P 1 B P EA	2	29-Dec-87		31-Dec-99		100	0	PROD
			U13,U36									

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-1 HI SPEED MEMORY BD 9100-1 UM: EA PC: 4 ECN: 1011 ASSEMBLY QTY: 1
ERC: Z SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 13-Jun-89

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0098	200032010		IC 2-INPUT NAND 74LS38PC									
			IC	P 1 B P EA	1	14-Jul-87		31-Dec-99		100	0	PROD
			U3									
0090	200041138		IC MUX/DE-MUX SN74S138									
			IC	P 1 B P EA	1	31-Mar-86		31-Dec-99		100	0	PROD
			U59									
0084	200071007		IC BUFFER SN74LS244N									
			IC	P 1 B P EA	7	14-Jan-87		31-Dec-99		100	0	PROD
			U14,U66,U67,U68,U80									
			U81,U82									
0087	200071245		IC BUS XCEIVER SN74LS245N									
			IC	P 1 B P EA	6	14-Jan-87		31-Dec-99		100	0	PROD
			U46,U47,U76,U77,U86									
			U87									
0088	200071377		IC 8XFLOP W/ENABL 74LS377									
			IC	P 1 B P EA	3	14-Jan-87		31-Dec-99		100	0	PROD
			U90,U105,U106									
0068	200330002		IC 2-IN NOR GATE 74F02									
			IC	P 1 B P EA	2	31-Mar-86		31-Dec-99		100	0	PROD
			U37,U38									
0067	200330004		IC FAST HEX INV 74F04									
			IC	P 1 B P EA	2	29-Dec-87		31-Dec-99		100	0	PROD
			U2,U32									
0029	200330008		IC 2-INPUT AND GATE 74F08									
			IC	P 1 B P EA	2	14-Jan-87		31-Dec-99		100	0	PROD
			U6,U101									
0065	200330010		IC 3-INPUT NAND 74F10									
			IC	P 1 B P EA	1	27-Mar-86		31-Dec-99		100	0	PROD
			U17									
0030	200330020		IC 4-IN NAND GATE 74F20									
			IC	P 1 B P EA	1	01-Jan-70		31-Dec-99		100	0	PROD
			U16									
0096	200330032		IC 2-INPUT OR 74F32									
			IC	P 1 B P EA	1	14-Jan-87		31-Dec-99		100	0	PROD
			U10									
0063	200332011		IC 3-IN AND GATE 74F11									
			IC	P 1 B P EA	2	27-Mar-86		31-Dec-99		100	0	PROD
			U9,U28									
0066	200340074		IC D-TYPE POS FLOP 74F74									
			IC	P 1 B P EA	2	02-Sep-86		31-Dec-99		100	0	PROD
			U4,U7									
0085	200340139		IC DECODER/DEMUX SN74S139									
			IC	P 1 B P EA	1	31-Mar-86		31-Dec-99		100	0	PROD
			U53									
0002	200344105		IC 2-3-2-IN OR/NOR 10H105									
			IC	P 1 B P EA	1	02-Sep-86		31-Dec-99		100	0	PROD
			U98									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-1 HI SPEED MEMORY BD 9100-1 UM: EA PC: 4 ECN: 1011 ASSEMBLY QTY: 1
ERC: Z SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 13-Jun-89

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0034	200344131		IC DUAL D M-S FLOP 10H131									
			IC	P 1 A P EA	2	14-Jan-87		31-Dec-99		100	0	PROD
			U96,U97									
0077	200370377		IC OCTAL D FLOP 74F377									
		4	IC	P 1 B P EA	7	14-Jan-87		31-Dec-99		100	0	PROD
			U23,U24,U48,U56,U57									
			U64,U65									
0035	200371374		IC D-TYP FLOP 74F374PC									
			IC	P 1 A P EA	4	01-Jan-70		31-Dec-99		100	0	PROD
			U18,U19,U20,U21									
0061	200441161		IC 4-BIT COUNTER 74F161									
			IC	P 1 B P EA	10	27-Mar-86		31-Dec-99		100	0	PROD
			U22,U25,U33,U34,U35									
			U49,U50,U102,U103,									
			U104									
0038	200570521		IC 8BIT COMPARATOR 74F521									
			IC	P 1 B P EA	2	27-Mar-86		31-Dec-99		100	0	PROD
			U55,U58									
0039	204042007		IC QUAD TRANSL MC10124P									
			IC	P 1 A P EA	10	02-Sep-86		31-Dec-99		100	0	PROD
			U42,U43,U44,U45,U72									
			U73,U74,U75,U93,U94									
0094	205271064		IC 8K X 8 RAM 7164S									
		4	IC	P 1 A P EA	8	13-Jun-89		31-Dec-99		100	0	PROD
			U40,U41,U62,U63,U70,									
			U71,U84,U85.									
0043	205280128		IC 2048X8 STATC RAM 7C128									
			IC	P 1 B P EA	2	27-Mar-86		31-Dec-99		100	0	PROD
			U78,U79									
0064	205630164		IC SHIFT REGISTER 74F164									
			IC	P 1 B P EA	1	27-Mar-86		31-Dec-99		100	0	PROD
			U8									
0070	207170541		IC BUFF/LINE DRIV 74LS541									
			IC	P 1 B P EA	1	27-Mar-86		31-Dec-99		100	0	PROD
			U60									
0086	207171240		IC 3-STATE BUFFER 74S240									
			IC	P 1 B P EA	3	31-Mar-86		31-Dec-99		100	0	PROD
			U61,U69,U83									
0069	207171244		IC FAST OCTAL BUFF 74F244									
			IC	P 1 B P EA	2	27-Mar-86		31-Dec-99		100	0	PROD
			U88,U89									
0040	207244125		IC QUAD MECL-TTL 10H125									
			IC	P 1 B P EA	1	06-Oct-87		31-Dec-99		100	0	PROD
			U99									
0031	207340174		IC 4-TO-1 MULTIPLX 10174									
		4	IC	P 1 B P EA	1	02-Sep-86		31-Dec-99		100	0	PROD
			U95									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-1 HI SPEED MEMORY BD 9100-1 UM: EA PC: 4 ECN: 1011 ASSEMBLY QTY: 1
ERC: Z SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 13-Jun-89

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0071	207470640		IC BUS TRANSCEIVER LS640										
			IC	U91,U107	P 1 B P EA	2	27-Mar-86		31-Dec-99		100	0	PROD
0056	290130010		DELAY LINE 10 N-SEC										
			DELA	U92	P 1 B P EA	1	14-Jul-87		31-Dec-99		100	0	PROD
0081	300050001		CHOKE FERRITE SINGLE LEAD										
			INDU	L1,L2	P 1 A P EA	2	14-Jul-87		31-Dec-99		100	0	PROD
0078	402610005		CONN CO-AX PC MTG SMB										
		4	CONN	J112	P 1 A P EA	1	19-May-89		31-Dec-99		100	0	PROD
0052	403170026		HDR DBL ROW RT ANGL 26										
			CONN	J117	P 1 B P EA	1	01-Jan-70		31-Dec-99		100	0	PROD
0053	403170034		HDR DBL ROW RT ANGL 34										
			CONN	J115,J116	P 1 B P EA	2	01-Jan-70		31-Dec-99		100	0	PROD
0105	403181003		HDR SINGL ROW 3										
			CONN		P 1 B P EA	1	26-Feb-88		31-Dec-99		100	0	PROD
0099	403950002		POLARIZING KEY										
			SOCK		P 1 B P EA	6	10-Jun-87		31-Dec-99		100	0	PROD
0079	408110008		TERMINAL DOUBLE TURRET										
			CONN		P 1 B P EA	6	02-Sep-86		31-Dec-99		100	0	PROD
0057	433222005		FUSE PICO II 125V 2 AMP										
			FUSE	F2	P 1 B P EA	1	14-Jul-87		31-Dec-99		100	0	PROD
0083	433225001		FUSE PICO II 125V 5 AMP										
			FUSE	F1	P 1 B P EA	1	14-Jul-87		31-Dec-99		100	0	PROD
0101	454318012		HDR SOLD TAIL/MALE 12										
		4	CONN		P 1 B P EA	1	01-Sep-87		31-Dec-99		100	0	PROD
0100	454370002		SHUNT 2 POS										
			SOCK		P 1 B P EA	2	12-May-88		31-Dec-99		100	0	PROD
0060	719100013		PC BD PREASS'Y 9100-1										
		4	PCB		P 1 A P EA	1	01-Jan-70		31-Dec-99		100	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0167	102412100		CAP CERA DISC 100V 10 PF														
			CAP C147,C142	P	1		B	P	EA	2	31-Aug-87		31-Dec-99		100	0	PROD
0133	102412101		CAP CERA DISC 100V 100 PF														
			CAP C135,C137	P	1		B	P	EA	2	23-Oct-87		31-Dec-99		100	0	PROD
0237	102412181		CAP CERA DISC 100V 180 PF														
			CAP C231,C235	P	1		B	P	EA	2	29-Mar-89		31-Dec-99		100	0	PROD
0233	102412270		CAP CERA DISC 100V 27 PF														
			CAP C63	P	1		B	P	EA	1	11-Aug-88		31-Dec-99		100	0	PROD
0164	102412470		CAP CERA DISC 100V 47 PF														
			CAP C187,C219,C228,C233	P	1		B	P	EA	4	16-Feb-89		31-Dec-99		100	0	PROD
0182	102412820		CAP CERA DISC 100V 82 PF														
			CAP C55	P	1		B	P	EA	1	23-Oct-87		31-Dec-99		100	0	PROD
0230	103427104		CAP CERA MONO 100V .1 UF														
			CAP C56	P	1		A	P	EA	1	28-Mar-88		31-Dec-99		100	0	PROD
0183	106415102		CAP CERA MONO 100V .001UF														
		4	CAP C101,C114,C154,C222	P	1		B	P	EA	4	21-Sep-90		31-Dec-99		100	0	PROD
0011	106415103		CAP CERA MONO 100V .01UF														
		4	CAP	P	1		B	P	EA	130	21-Sep-90		31-Dec-99		100	0	PROD
0180	142224476		CAP TANT DIP CASE 47 UF														
			CAP C57,C139A,C5,C64,C60	P	1		B	P	EA	5	23-Oct-87		31-Dec-99		100	0	PROD
0021	142824685		CAP TANT DIP CASE 6.8 UF														
			CAP C204,C205,C42,C43 C44,C230	P	1		A	P	EA	7	14-Apr-88		31-Dec-99		100	0	PROD
0120	146424106		CAP MINI ALUM 20% 10 UF														
			CAP	P	1		B	P	EA	43	14-Apr-88		31-Dec-99		100	0	PROD
0075	147674102		CAP ALU METAL CAN 1000 UF														
			CAP C169,C172,C170,C166	P	1		B	P	EA	4	18-May-87		31-Dec-99		100	0	PROD
0206	158819001		CAP VARI CERA 3.5 - 18 PF														
			CAP	P	1		B	P	EA	3	23-Nov-87		31-Dec-99		100	0	PROD
0008	161030000		RES COMP ZERO OHMS														
			RES R182,R23,R24,R26	P	1		B	P	EA	4	23-Oct-87		31-Dec-99		100	0	PROD
0210	161225101		RES CARBON FILM 100 OHMS														
			RES R89	P	1		B	P	EA	1	23-Mar-88		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0072	161225102		RES CARBON FILM 1 K									
			RES	P 1 B P EA	6	16-Dec-87		31-Dec-99		100	0	PROD
			R121,R63,R111									
			R82,R134,R6									
0015	161225112		RES CARBON FILM 1.1 K									
			RES	P 1 B P EA	1	09-Jun-87		31-Dec-99		100	0	PROD
			R136									
0170	161225151		RES CARBON FILM 150 OHMS									
			RES	P 1 B P EA	2	31-Aug-87		31-Dec-99		100	0	PROD
			R148,R154									
0196	161225152		RES CARBON FILM 1.5 K									
			RES	P 1 B P EA	1	18-Nov-87		31-Dec-99		100	0	PROD
			R4									
0030	161225162		RES CARBON FILM 1.6 K									
			RES	P 1 B P EA	4	09-Jun-87		31-Dec-99		100	0	PROD
			R14,R17,R19,R5									
0190	161225201		RES CARBON FILM 200 OHMS									
			RES	P 1 B P EA	1	23-Oct-87		31-Dec-99		100	0	PROD
			R164									
0040	161225202		RES CARBON FILM 2 K									
			RES	P 1 B P EA	16	23-Oct-87		31-Dec-99		100	0	PROD
			R21,R15,R16,R18,R34									
			R93,R94,R45,R160,R86									
			R87,R107,R108,R195									
			R90,R211									
0111	161225243		RES CARBON FILM 24 K									
			RES	P 1 B P EA	2	09-Jun-87		31-Dec-99		100	0	PROD
			R179,R178									
0229	161225244		RES CARBON FILM 240 K									
			RES	P 1 B P EA	1	28-Mar-88		31-Dec-99		100	0	PROD
			R163									
0204	161225272		RES CARBON FILM 2.7 K									
			RES	P 1 B P EA	1	18-Nov-87		31-Dec-99		100	0	PROD
			R3									
0063	161225302		RES CARBON FILM 3 K									
			RES	P 1 B P EA	4	23-Oct-87		31-Dec-99		100	0	PROD
			R22,R20,R25,R27									
0189	161225330		RES CARBON FILM 33 OHMS									
			RES	P 1 B P EA	4	23-Oct-87		31-Dec-99		100	0	PROD
			R155,R156,R146,R147									
0017	161225363		RES CARBON FILM 36 K									
			RES	P 3 B P EA	2	02-Jun-87		31-Dec-99		100	0	PROD
			R81,R110									
0065	161225391		RES CARBON FILM 390 OHMS									
			RES	P 1 B P EA	14	23-Oct-87		31-Dec-99		100	0	PROD
			R84,R85,R115-R120									
			R58,R88,R107,R88A									
			R89B,R197									

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / CODE / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0073	161225431		RES CARBON FILM 430 OHMS														
			RES		P	1	B	P	EA	3	23-Oct-87		31-Dec-99		100	0	PROD
			R109,R83,R159														
0213	161225471		RES CARBON FILM 470 OHMS														
			RES		P	1	B	P	EA	1	16-Dec-87		31-Dec-99		100	0	PROD
			R7														
0024	161225510		RES CARBON FILM 51 OHMS														
			RES		P	1	B	P	EA	4	23-Mar-88		31-Dec-99		100	0	PROD
			R1,R2,R91,R75														
0134	161225512		RES CARBON FILM 5.1 K														
			RES		P	1	B	P	EA	6	23-Oct-87		31-Dec-99		100	0	PROD
			R114,R55,R78,R95														
			R76,R77														
0054	161225513		RES CARBON FILM 51 K														
			RES		P	1	B	P	EA	1	02-Jun-87		31-Dec-99		100	0	PROD
			R133														
0047	161225562		RES CARBON FILM 5.6 K														
			RES		P	1	B	P	EA	1	02-Jun-87		31-Dec-99		100	0	PROD
			R135														
0069	161225622		RES CARBON FILM 6.2 K														
			RES		P	1	B	P	EA	1	02-Jun-87		31-Dec-99		100	0	PROD
			R132														
0186	161225682		RES CARBON FILM 6.8 K														
			RES		P	1	B	P	EA	1	23-Oct-87		31-Dec-99		100	0	PROD
			R162														
0184	161225751		RES CARBON FILM 750 OHMS														
			RES		P	1	B	P	EA	1	23-Oct-87		31-Dec-99		100	0	PROD
			R161														
0074	161335047		RES CARBON FILM 4.7 OHMS														
			RES		P	1	B	P	EA	6	23-Oct-87		31-Dec-99		100	0	PROD
			R79,R80,R112,R113														
			R157,R158														
0165	161335100		RES CARBON FILM 10 OHMS														
			RES		P	1	B	P	EA	8	31-Aug-87		31-Dec-99		100	0	PROD
			R71,R72,R73,R74,R100														
			R101,R105,R106														
0192	161335102		RES CARBON FILM 1 K														
			RES		P	1	B	P	EA	1	23-Oct-87		31-Dec-99		100	0	PROD
			R122														
0214	161335201		RES CARBON FILM 200 OHMS														
			RES		P	1	B	P	EA	2	16-Dec-87		31-Dec-99		100	0	PROD
			R193,R194														
0215	168041279		RES ULTRA PREC 60.4 OHMS														
		4	RES		P	1	B	P	EA	6	30-Dec-87		31-Dec-99		100	0	PROD
			R68,R68A,R68B,R92														
			R92A,R92B														

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S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0217	168041439		RES ULTRA PREC 3.01 K														
		4	RES		P	1	B	P	EA	2	30-Dec-87		31-Dec-99		100	0	PROD
			R144,R153														
0218	168041445		RES ULTRA PREC 3.48 K														
		4	RES		P	1	B	P	EA	2	30-Dec-87		31-Dec-99		100	0	PROD
			R145,R150														
0219	168041457		RES ULTRA PREC 4.64 K														
			RES		P	1	B	P	EA	2	30-Dec-87		31-Dec-99		100	0	PROD
			R143,R149														
0143	168139393		RES RN55E .1% 1.0 K														
			RES		P	1	B	P	EA	2	23-Oct-87		31-Dec-99		100	0	PROD
			R128,R64														
0146	168139451		RES RN55E .1% 4.02 K														
		4	RES		P	1	B	P	EA	1	09-Jun-87		31-Dec-99		100	0	PROD
			R129														
0149	168139505		RES RN55E .1% 14.7 K														
		4	RES		P	1	B	P	EA	1	09-Jun-87		31-Dec-99		100	0	PROD
			R130														
0089	168139550		RES RN55E .1% 43.2 K														
		4	RES		P	1	B	P	EA	1	11-Jun-87		31-Dec-99		100	0	PROD
			R125														
0144	168139565		RES RN55E .1% 61.9 K														
		4	RES		P	1	B	P	EA	1	23-Oct-87		31-Dec-99		100	0	PROD
			R124														
0145	168139566		RES RN55E .1% 63.4 K														
		4	RES		P	1	B	P	EA	2	23-Oct-87		31-Dec-99		100	0	PROD
			R123,R65														
0138	168531201		RES PREC RN55D 10.0 OHMS														
			RES		P	1	B	P	EA	1	09-Jun-87		31-Dec-99		100	0	PROD
			R180														
0139	168531217		RES PREC RN55D 14.7 OHMS														
			RES		P	1	B	P	EA	1	09-Jun-87		31-Dec-99		100	0	PROD
			R181														
0086	168531268		RES PREC RN55D 49.9 OHMS														
			RES		P	3	B	P	EA	4	31-Aug-87		31-Dec-99		100	0	PROD
			R52,R63,R65,R89														
			R64														
0207	168531271		RES PREC RN55D 53.6 OHMS														
		4	RES		P	3	B	P	EA	1	23-Nov-87		31-Dec-99		100	0	PROD
			R64														
0195	168531285		RES PREC RN55D 75.0 OHMS														
			RES		P	1	B	P	EA	2	23-Oct-87		31-Dec-99		100	0	PROD
			R49A,R51A														
0078	168531297		RES PREC RN55D 100 OHMS														
			RES		P	1	B	P	EA	1	02-Jun-87		31-Dec-99		100	0	PROD
			R66														

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PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0156	168531305		RES PREC RN55D 121 OHMS									
			RES	P 1 B P EA	1	31-Aug-87		31-Dec-99		100	0	PROD
			R123A									
0026	168531314		RES PREC RN55D 150 OHMS									
			RES	P 3 B P EA	1	09-Jun-87		31-Dec-99		100	0	PROD
			R90									
0031	168531321		RES PREC RN55D 178 OHMS									
			RES	P 1 B P EA	2	23-Jul-86		31-Dec-99		100	0	PROD
			R9,R13									
0216	168531325		RES PREC RN55D 196 OHMS									
			RES	P 1 B P EA	2	30-Dec-87		31-Dec-99		100	0	PROD
			R99,R57									
0100	168531326		RES PREC RN55D 200 OHMS									
			RES	P 1 B P EA	6	30-Dec-87		31-Dec-99		100	0	PROD
			R53,R54,R56,R96-R98									
0036	168531329		RES PREC RN55D 215 OHMS									
			RES	P 1 B P EA	4	23-Oct-87		31-Dec-99		100	0	PROD
			R59-R62									
0102	168531335		RES PREC RN55D 249 OHMS									
			RES	P 1 B P EA	2	02-Jun-87		31-Dec-99		100	0	PROD
			R29,R33									
0043	168531343		RES PREC RN55D 301 OHMS									
			RES	P 1 B P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
			R11									
0105	168531369		RES PREC RN55D 562 OHMS									
			RES	P 1 B P EA	1	31-Aug-87		31-Dec-99		100	0	PROD
			R32									
0163	168531377		RES PREC RN55D 681 OHMS									
			RES	P 1 B P EA	1	31-Aug-87		31-Dec-99		100	0	PROD
			R67									
0194	168531381		RES PREC RN55D 750 OHMS									
			RES	P 1 B P EA	2	23-Oct-87		31-Dec-99		100	0	PROD
			R49,R51									
0042	168531389		RES PREC RN55D 909 OHMS									
			RES	P 1 B P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
			R10									
0087	168531401		RES PREC RN55D 1.21 K									
			RES	P 1 B P EA	1	25-Aug-86		31-Dec-99		100	0	PROD
			R28									
0104	168531402		RES PREC RN55D 1.24 K									
			RES	P 3 B P EA	1	31-Aug-87		31-Dec-99		100	0	PROD
			R31									
0032	168531411		RES PREC RN55D 1.54 K									
			RES	P 1 B P EA	2	23-Jul-86		31-Dec-99		100	0	PROD
			R8,R12									
0085	168531413		RES PREC RN55D 1.62 K									
			RES	P 1 B P EA	2	25-Aug-86		31-Dec-99		100	0	PROD
			R140,R142									

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PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY	PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0103	168531458		RES PREC RN55D 4.75 K																
			RES		P	3		B	P	EA	1		02-Jun-87		31-Dec-99		100	0	PROD
			R30																
0220	168531489		RES PREC RN55D 10.0 K																
			RES		P	1		B	P	EA	4		14-Apr-88		31-Dec-99		100	0	PROD
			R139,R141,R137,R138																
0025	180247101		RES VARI CERMET 100 OHMS																
			RES		P	1		B	P	EA	1		12-Sep-88		31-Dec-99		100	0	PROD
			R127																
0234	180247201		RES VARI CERMET 200 OHMS																
			RES		P	1		B	P	EA	1		12-Sep-88		31-Dec-99		100	0	PROD
			R126																
0225	190102001		RES NETWORK 220/330 OHMS																
			RES		P	1		B	P	EA	4		23-Mar-88		31-Dec-99		100	0	PROD
			U17,U18,U24,U25																
0039	190322332		RESISTOR NETWORK 3.3 K																
		4	RES		P	1		B	P	EA	1		09-Jun-87		31-Dec-99		100	0	PROD
			U33																
0033	190642101		RESISTOR NETWORK 100 OHMS																
			RES		P	1		B	P	EA	6		23-Mar-88		31-Dec-99		100	0	PROD
			U2,U28A,U28B																
			U29A,U29B,U26																
0203	190642560		RESISTOR NETWORK 56 OHMS																
			RES		P	1		B	P	EA	1		30-Oct-87		31-Dec-99		100	0	PROD
			U26A																
0199	190842302		RESISTOR NETWORK 3 K																
		4	RES		P	1		B	P	EA	1		26-Oct-87		31-Dec-99		100	0	PROD
			U31																
0200	190842332		RESISTOR NETWORK 3.3 K																
		4	RES		P	1		B	P	EA	1		26-Oct-87		31-Dec-99		100	0	PROD
			U32																
0177	200031005		IC HEX INVERTER SN7406N																
			IC		P	1		B	P	EA	1		23-Oct-87		31-Dec-99		100	0	PROD
			U15																
0009	200031046		IC HEX INVERTER SN74LS04N																
			IC		P	1		B	P	EA	1		23-Jul-86		31-Dec-99		100	0	PROD
			U13																
0188	200031051		IC 2-INPUT NOR SN74LS02N																
			IC		P	1		B	P	EA	2		23-Oct-87		31-Dec-99		100	0	PROD
			U11,U11A																
0119	200041032		IC 13-INPUT NAND SN74S133																
			IC		P	1		B	P	EA	1		02-Jun-87		31-Dec-99		100	0	PROD
			U16																
0178	200041044		IC MULTIVIBR SN74LS123N																
			IC		P	1		B	P	EA	1		23-Oct-87		31-Dec-99		100	0	PROD
			U62																

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PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0071	200071007		IC BUFFER SN74LS244N										
				IC	P 1 B P EA	1	14-Aug-86		31-Dec-99		100	0	PROD
				U63									
0068	200071377		IC 8XFLOP W/ENABL 74LS377										
				IC	P 1 B P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
				U50									
0115	200131009		IC QUAD AND GT SN74LS09N										
				IC	P 1 B P EA	1	02-Jun-87		31-Dec-99		100	0	PROD
				U43									
0116	200330008		IC 2-INPUT AND GATE 74F08										
				IC	P 1 B P EA	1	02-Jun-87		31-Dec-99		100	0	PROD
				U34									
0027	200340074		IC D-TYPE POS FLOP 74F74										
				IC	P 1 B P EA	2	09-Jun-87		31-Dec-99		100	0	PROD
				U61,U42									
0007	200341138		IC DECODER DM74LS138										
				IC	P 1 B P EA	2	23-Jul-86		31-Dec-99		100	0	PROD
				U12,U14									
0020	200344102		IC QUAD 2-IN NOR 10H102										
				IC	P 1 B P EA	2	18-May-87		31-Dec-99		100	0	PROD
				U1,U3									
0117	200371273		IC OCTAL D-FLOP 74F273										
				IC	P 1 B P EA	2	23-Oct-87		31-Dec-99		100	0	PROD
				U51,U64									
0006	205632164		IC 8-BIT SHIFT REG HC164										
		4		IC	P 1 B P EA	4	23-Jul-86		31-Dec-99		100	0	PROD
				U6,U8,U9,U10									
0013	207250574		IC 12-BIT ADC AD574ALD										
		4		IC	P 1 A P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
				U49									
0205	207272232		IC 12-BIT DAC MP1230KN										
		4		IC	P 1 B P EA	2	19-Nov-87		31-Dec-99		100	0	PROD
				U56,U58									
0016	207277528		IC DUAL 8-BIT DAC 7528										
				IC	P 1 B P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
				U54									
0001	207340508		IC 8-CH ANALOG MPLX DG508										
				IC	P 1 B P EA	2	18-May-87		31-Dec-99		100	0	PROD
				U47,U48									
0012	207470640		IC BUS TRANSCEIVER LS640										
				IC	P 1 B P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
				U65									
0010	208031010		IC QUAD DIFF COMP LM339N										
				IC	P 1 B P EA	2	31-Aug-87		31-Dec-99		100	0	PROD
				U5,U7									
0070	208100103		IC OP AMP CL103										
		4		IC	P 1 A P EA	2	18-May-87		31-Dec-99		300	0	PROD
				U37,U38									
				GIVE TO SSD MANU									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0014	208110007		IC LO OFFSET OP AMP OP-07									
			IC	P 1 B P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
			U46									
0003	208110353		IC DUAL OP AMP LF353N									
			IC	P 1 B P EA	2	26-Jan-89		31-Dec-99		100	0	PROD
			U52,U53									
0236	208110412		IC OP AMP J-FET LF412									
		4	IC	P 3 B P EA	2	07-Feb-89		31-Dec-99		100	0	PROD
			U55,U57									
0056	208122337		IC ADJ -VOLT REG LM337T									
			IC	P 1 B P EA	3	09-Jun-87		31-Dec-99		100	0	PROD
			VR1,VR2,VR4									
0148	208213002		IC VOLT REF +5V REF-02									
		4	IC	P 1 B P EA	1	09-Jun-87		31-Dec-99		100	0	PROD
			U45									
0057	208510317		IC ADJ +V REG 317LZ									
			IC	P 1 B P EA	3	02-Jun-87		31-Dec-99		100	0	PROD
			VR5,VR6,VR7									
0055	208570317		IC ADJ +V REG LM317									
			IC	P 1 B P EA	1	23-Jul-86		31-Dec-99		100	0	PROD
			VR3									
0018	208650393		IC DUAL VOLT COMP LM393N									
			IC	P 1 B P EA	3	23-Oct-87		31-Dec-99		100	0	PROD
			U41,U44,U60									
0197	229020055		TRANS VOLT SUPPR P6KE6.8									
			XIST	P 1 B P EA	2	23-Oct-87		31-Dec-99		100	0	PROD
			CR7,CR8									
0084	229020089		TRANS VOLT SUPPR P6KE11									
			XIST	P 1 B P EA	4	18-May-87		31-Dec-99		100	0	PROD
			CR5,CR10,CR17,CR22									
0022	230110005		DIODE SWITCHING 1N4448									
			DIOD	P 1 B P EA	10	23-Oct-87		31-Dec-99		100	0	PROD
			CR6,CR9,CR16,CR18									
			CR33,CR4,CR3,CR14									
			CR15									
0023	235010005		DIODE RECTIFIER 1N4005									
			DIOD	P 1 B P EA	5	18-May-87		31-Dec-99		100	0	PROD
			CR11,CR12,CR20,CR21									
			CR1									
0118	240035341		DIODE ZENER 6.2V 1N5341B									
			DIOD	P 1 B P EA	1	02-Jun-87		31-Dec-99		100	0	PROD
			CR2									
0046	253012811		DIODE SCHOTTKY HP2811									
		4	DIOD	P 1 D P EA	3	04-Jun-90		31-Dec-99		100	0	PROD
0049	270110003		TRANSISTOR NPN PN2222A									
			XIST	P 1 B P EA	5	23-Mar-88		31-Dec-99		100	0	PROD
			Q4-Q6,Q7A,Q8A									

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PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0227	270170001		TRANSISTOR NPN 2N5770														
			XIST		P	1	B	P	EA	2	23-Mar-88		31-Dec-99		100	0	PROD
			Q2,Q3														
0158	275110001		TRANSISTOR PNP 2N2907A														
			XIST		P	1	B	P	EA	2	31-Aug-87		31-Dec-99		100	0	PROD
			Q7,Q8														
0060	300030001		BEAD SHIELDING FERRITE														
			INDU		P	1	B	P	EA	2	23-Oct-87		31-Dec-99		100	0	PROD
			L3,L4														
0059	300050001		CHOKE FERRITE SINGLE LEAD														
			INDU		P	1	A	P	EA	8	09-Jun-87		31-Dec-99		100	0	PROD
			L5,L6,L7,L8,L9,L10														
			L1,L2														
0052	402610005		CONN CO-AX PC MTG SMB														
		4	CONN		P	1	A	P	EA	2	19-May-89		31-Dec-99		100	0	PROD
			J213,J214														
0076	402610006		CONN CO-AX PC MTG SMB														
			CONN		P	1	B	P	EA	3	19-May-89		31-Dec-99		100	0	PROD
			J205,J206,J207														
0053	403170034		HDR DBL ROW RT ANGL 34														
			CONN		P	1	B	P	EA	2	23-Jul-86		31-Dec-99		100	0	PROD
			J6,J7														
0228	403181002		HDR SINGL ROW STRAIGHT 2														
			CONN		P	1	B	P	EA	2	23-Mar-88		31-Dec-99		100	0	PROD
0198	403950002		POLARIZING KEY														
			SOCK		P	1	B	P	EA	4	23-Oct-87		31-Dec-99		100	0	PROD
0209	405764112		SOCKET SINGLE WIRE 12-POS														
			SOCK		P	1	B	P	EA	8	23-Mar-88		31-Dec-99		100	0	PROD
0041	408110008		TERMINAL DOUBLE TURRET														
			CONN		P	1	B	P	EA	7	11-Jun-87		31-Dec-99		100	0	PROD
0176	430542712		RELAY 2 FORM C DPDT														
		4	RELA		P	1	A	P	EA	12	21-Oct-87		31-Dec-99		100	0	PROD
			K1-K12														
0064	433220002		FUSE PICO II 125V 3 AMP														
			FUSE		P	1	B	P	EA	3	23-Oct-87		31-Dec-99		100	0	PROD
			F2-F4														
0187	433225001		FUSE PICO II 125V 5 AMP														
			FUSE		P	1	B	P	EA	1	23-Oct-87		31-Dec-99		100	0	PROD
			F1														
0131	454368024		HEADER (PLUG STRIP) 24														
			CONN		P	1	B	P	EA	1	09-Jun-87		31-Dec-99		100	0	PROD
0037	500860302		INSULATOR FOR TO-220														
			DIOD		P	1	A	P	EA	4	14-Aug-86		31-Dec-99		100	0	PROD
			VR1-VR4														
0034	505070002		HEAT SINK FOR TO-220														
			HEAT		P	1	B	P	EA	4	14-Aug-86		31-Dec-99		100	0	PROD
			VR1-VR4														

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0226	505112140		HEAT SINK														
			HEAT	P	1		B	P	EA	4	23-Mar-88		31-Dec-99		100	0	PROD
0201	521440020		SPACER HEX 4-40X5/8														
			HDWR	P	1		B	P	EA	3	27-Oct-87		31-Dec-99		100	0	PROD
0202	555100008		STANDOFF .125 LONG														
		4	HDWR	P	1		B	P	EA	4	30-Oct-87		31-Dec-99		100	0	PROD
0151	555462002		NUT SELF-CLINCHING 4-40														
			HDWR	P	1		B	P	EA	4	23-Oct-87		31-Dec-99		100	0	PROD
0088	560440004		SCREW PHILIPS 4-40X1/4														
			HDWR	P	1		B	P	EA	7	30-Oct-86		31-Dec-99		100	0	PROD
0172	560440006		SCREW PHILIPS 4-40X3/8														
			HDWR	P	1		B	P	EA	4	07-Oct-87		31-Dec-99		300	0	PROD
			GIVE TO SSD MANU.														
0038	574409005		WASHER SHOULDER NYLON #4														
			HDWR	P	1		B	P	EA	4	14-Aug-86		31-Dec-99		100	0	PROD
0175	581440001		NUT HEX SMALL OD SIZE 4														
			HDWR	P	1		B	P	EA	7	07-Oct-87		31-Dec-99		100	0	PROD
0153	591692330		WIRE BLU/WHT TW PR SOLID AWG 30														
			WIRE	P	1		B	P	EA	0.300000	12-Jun-87		31-Dec-99		100	0	PROD
0171	709100023		SHIELD FOR 9100-2														
		4	FAB	P	1		B	P	EA	1	07-Oct-87		31-Dec-99		300	0	FAB
			GIVE TO SSD MANU.														
0061	719100002		PC BD PREASS'Y 9100-2														
		4	PCB	P	1		A	P	EA	1	23-Jul-86		31-Dec-99		100	0	FAB
			REV F														
0235	CH599043013		HEAT SINK EPOXY														
			CHEM	P	1		B	P	EA	0	05-Dec-88		31-Dec-99		100	0	PROD
0099	HAT100	C	UNCASED CIRCUIT HAT100														
		4	HYB	A	1		C	P	EA	2	19-May-87		31-Dec-99		100	4	SSDSUB
			U39,U40														
0019	HFA100	J	HYB SIGNAL COND HFA100														
		4	HYB	A	1		B	P	EA	2	19-May-87		31-Dec-99		300	4	SSDSUB
			U35,U36														
			GIVE TO SSD MANU.														
0050	SM205624141		IC 8-BIT SHIFT REG 100141														
			IC	P	1		A	P	EA	4	18-May-87		31-Dec-99		100	0	PROD
			U19,U20,U22,U23														
0051	SM207124112		IC QUAD LINE DRIVER 112														
			IC	P	1		B	P	EA	1	18-May-87		31-Dec-99		100	0	PROD
			U21														
0094	SM207232108		IC 8-BIT DAC BT108														
		4	IC	P	1		A	P	EA	2	18-May-87		31-Dec-99		100	0	PROD
			U27,U30														
0223	SM653181269		RES THICK FILM 1% 51.1 OHMS														
			RES	P	1		B	P	EA	4	03-Mar-88		31-Dec-99		100	0	PROD
			R39,R40,R41,R42														

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-2 ANALOG BD UM: EA PC: 4 ECN: 1016 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / CODE / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0224	SM653181285		RES THICK FILM 1% 75 OHMS														
			RES		P	1		B	P	EA 2	03-Mar-88		31-Dec-99		100	0	PROD
			R198,R199														
0221	SM653181297		RES THICK FILM 1% 100 OHMS														
			RES		P	1		B	P	EA 8	18-Feb-88		31-Dec-99		100	0	PROD
			R35,R36,R37,R38,R43 R44,R46,R47														
0222	SM653181301		RES THICK FILM 1% 110 OHMS														
			RES		P	1		B	P	EA 2	03-Mar-88		31-Dec-99		100	0	PROD
			R48,R50														
0096	SM661178104		CAP CERA CHIP .1 UF														
			CAP		P	1		B	P	EA 2	02-Jun-87		31-Dec-99		100	0	PROD
			C70,C81														
0211	SM661186330		CAP CERA CHIP 10% 33 PF														
			CAP		P	1		B	P	EA 3	12-Jul-88		31-Dec-99		100	0	PROD
			C224,C226,C234														
0212	SM661186820		CAP CERA CHIP 10% 82 PF														
		4	CAP		P	1		B	P	EA 2	23-Nov-87		31-Dec-99		100	0	PROD
			C223,C225														
0232	SM661286102		CAP CERA CHIP 10% .001 UF														
			CAP		P	1		B	P	EA 5	12-Jul-88		31-Dec-99		100	0	PROD
			C79,C90,C227-C229														
0097	SM661286103		CAP CERA CHIP 10% .01 UF														
			CAP		P	1		A	P	EA 25	12-Jul-88		31-Dec-99		100	0	PROD
			C65-C69,C71-C73,C77, C80,C80A,C86-C89, C91,C91A,C103,C104, C107,C116,C173,C220, C223,C234														

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-3 SRAM/GPIB/FP PORT 9100-3 UM: EA PC: 4 ECN: 1008 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 12-Oct-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE / COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0003	103327103		CAP CERA MONO 50V .01 UF CAP	P 1 A P EA	56	11-Sep-86		31-Dec-99		600	0	PROD
0007	142564107	4	CAP TANT DIP CASE 100UF CAP C5,C6,C10,C11	P 1 B P EA	5	12-Oct-88		31-Dec-99		600	0	PROD
0006	142824685		CAP TANT DIP CASE 6.8 UF CAP C1,C2,C3,C4,C12,C13 C14	P 1 A P EA	7	15-Jul-87		31-Dec-99		600	0	PROD
0095	142864476	4	CAP TANT DIP CASE 47 UF CAP C8,C9	P 1 B P EA	2	12-Oct-88		31-Dec-99		600	0	PROD
0085	161225101		RES CARBON FILM 100 OHMS RES R36,R37	P 1 B P EA	2	29-Sep-87		31-Dec-99		600	0	PROD
0093	161225102		RES CARBON FILM 1 K RES R48,R46	P 1 B P EA	2	29-Sep-87		31-Dec-99		600	0	PROD
0001	161225103		RES CARBON FILM 10 K RES R4,R9,R11,R12,R13 R14,R15,R16,R18.R19	P 1 B P EA	10	10-Sep-87		31-Dec-99		600	0	PROD
0014	161225222		RES CARBON FILM 2.2 K RES R10,R30,R33	P 1 B P EA	3	15-Jul-87		31-Dec-99		600	0	PROD
0090	161225226	4	RES CARBON FILM 22 MEG RES R45,R44	P 1 B P EA	2	29-Sep-87		31-Dec-99		600	0	PROD
0094	161225472		RES CARBON FILM 4.7 K RES R47	P 1 B P EA	1	14-Oct-87		31-Dec-99		600	0	PROD
0067	161225512		RES CARBON FILM 5.1 K RES R26,R27	P 1 B P EA	2	15-Jul-87		31-Dec-99		600	0	PROD
0066	161225821		RES CARBON FILM 820 OHMS RES R32,R35	P 1 B P EA	2	15-Jul-87		31-Dec-99		600	0	PROD
0084	161335152		RES CARBON FILM 1.5 K RES R22,R23	P 1 B P EA	2	24-Aug-87		31-Dec-99		600	0	PROD
0064	161445300		RES CARBON FILM 30 OHMS RES R21,R20	P 1 B P EA	2	15-Jul-87		31-Dec-99		600	0	PROD
0069	168531489		RES PREC RN55D 10.0 K RES R24,R25,R28,R29	P 1 B P EA	4	15-Jul-87		31-Dec-99		600	0	PROD

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-3 SRAM/GPIB/FP PORT 9100-3 UM: EA PC: 4 ECN: 1008 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 12-Oct-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0065	180247102		RES VARI CERMET 1 K									
			RES	P 1 B P EA	2	15-Jul-87		31-Dec-99		600	0	PROD
			R31,R34									
0009	200031019		IC SHIFT REGIST SN74164N									
			IC	P 1 B P EA	1	11-Sep-86		31-Dec-99		600	0	PROD
			U33									
0016	200031032		IC HEX BUFF/DRIV SN7407N									
			IC	P 1 B P EA	1	01-Jan-70		31-Dec-99		600	0	PROD
			U48									
0059	200031044		IC 5-INPUT NOR SN74S260N									
			IC	P 1 B P EA	1	30-Apr-86		31-Dec-99		600	0	PROD
			U38									
0013	200330000		IC 2-INPUT NAND 74F00									
			IC	P 1 B P EA	1	27-Jan-87		31-Dec-99		600	0	PROD
			U32									
0058	200330002		IC 2-IN NOR GATE 74F02									
			IC	P 1 B P EA	1	27-Jan-87		31-Dec-99		600	0	PROD
			U40									
0052	200330008		IC 2-INPUT AND GATE 74F08									
			IC	P 1 B P EA	2	27-Jan-87		31-Dec-99		600	0	PROD
			U30,U36									
0057	200330010		IC 3-INPUT NAND 74F10									
			IC	P 1 B P EA	1	27-Jan-87		31-Dec-99		600	0	PROD
			U39									
0051	200330032		IC 2-INPUT OR 74F32									
			IC	P 1 B P EA	2	27-Jan-87		31-Dec-99		600	0	PROD
			U37,U41									
0054	200330086		IC EX-OR GATE 74F86									
			IC	P 1 B P EA	1	27-Jan-87		31-Dec-99		600	0	PROD
			U28									
0050	200340074		IC D-TYPE POS FLOP 74F74									
			IC	P 1 B P EA	1	27-Jan-87		31-Dec-99		600	0	PROD
			U35									
0053	200340138		IC 1-OF-8 DECODER 74F138									
			IC	P 1 B P EA	1	27-Jan-87		31-Dec-99		600	0	PROD
			U29									
0010	200342138		IC 3-TO-8 LN DEC 74HC138									
			IC	P 1 B P EA	2	11-Sep-86		31-Dec-99		600	0	PROD
			U17,U18									
0011	205270256		IC 32K X 8 RAM 62256									
			IC	P 1 B P EA	16	11-Sep-86		31-Dec-99		600	0	PROD
			U1-U16									
0060	207171244		IC FAST OCTAL BUFF 74F244									
			IC	P 1 B P EA	1	27-Jan-87		31-Dec-99		600	0	PROD
			U44									
0061	207173240		IC BUFF/LINE DRVR 74F240									
			IC	P 1 B P EA	3	27-Jan-87		31-Dec-99		600	0	PROD
			U45,U46,U47									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-3 SRAM/GPIB/FP PORT 9100-3 UM: EA PC: 4 ECN: 1008 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 12-Oct-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION / COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0032	207470160		IC BUS TRANSCEIVER 75160B									
			IC	P 1 A P EA	1	01-Jan-70		31-Dec-99		600	0	PROD
			U21									
0062	207470640		IC BUS TRANSCEIVER LS640									
			IC	P 1 B P EA	3	30-Apr-86		31-Dec-99		600	0	PROD
			U42,U49,U50									
0034	207490162		IC OCTAL BUS XCVR 75162A									
			IC	P 1 B P EA	1	01-Jan-70		31-Dec-99		600	0	PROD
			U20									
0071	208011008		IC VOLT COMPARATOR LM311N									
			IC	P 1 B P EA	2	15-Jul-87		31-Dec-99		600	0	PROD
			U53,U54									
0070	208031084		IC QUAD J-FET OP AMP 084									
			IC	P 1 B P EA	2	15-Jul-87		31-Dec-99		600	0	PROD
			U52,U55									
0072	208213002		IC VOLT REF +5V REF-02									
		4	IC	P 1 B P EA	1	15-Jul-87		31-Dec-99		600	0	PROD
			U51									
0037	227799914		IC GPIB CONTROL TMS9914A									
			IC	P 1 A P EA	1	01-Jan-70		31-Dec-99		600	0	PROD
			U26									
0021	230110005		DIODE SWITCHING 1N4448									
			DIOD	P 1 B P EA	5	14-Oct-87		31-Dec-99		600	0	PROD
			CR4,CR5,CR13,CR14									
			CR15									
0075	240425746		DIODE ZENER 3.3V 1N746A									
			DIOD	P 1 B P EA	1	15-Jul-87		31-Dec-99		600	0	PROD
			CR6									
0087	253050817		DIODE HOT CARRIER 1N5817									
			DIOD	P 1 B P EA	2	29-Sep-87		31-Dec-99		600	0	PROD
			CR17,CR18									
0088	270110001		TRANSISTOR NPN PN2369A									
			XIST	P 1 B P EA	2	29-Sep-87		31-Dec-99		600	0	PROD
			Q6,Q9									
0078	270110003		TRANSISTOR NPN PN2222A									
			XIST	P 1 B P EA	1	15-Jul-87		31-Dec-99		600	0	PROD
			Q1									
0089	275170001		TRANSISTOR PNP 2N5087									
			XIST	P 1 B P EA	2	29-Sep-87		31-Dec-99		600	0	PROD
			Q7,Q8									
0074	280170104		TRANSISTOR FET N VN0104N3									
			XIST	P 1 A P EA	1	15-Jul-87		31-Dec-99		600	0	PROD
			Q2									
0073	281170104		TRANSISTOR FET P VP0104N3									
			XIST	P 1 B P EA	3	10-Sep-87		31-Dec-99		600	0	PROD
			Q3,Q4,Q5									

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-3 SRAM/GPIB/FP PORT 9100-3 UM: EA PC: 4 ECN: 1008 ASSEMBLY QTY: 1
ERC: R SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 12-Oct-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE / COM.CD	S T S A P C Y P B L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0079	300050001		CHOKE FERRITE SINGLE LEAD										
			INDU	P 1 A P	EA	4	15-Jul-87		31-Dec-99		600	0	PROD
			L1,L2,L3,L4										
0042	403170026		HDR DBL ROW RT ANGL 26										
			CONN	P 1 B P	EA	2	30-Apr-86		31-Dec-99		600	0	PROD
			J1,J2										
0063	403950002		POLARIZING KEY										
			SOCK	P 1 B P	EA	4	10-Jun-87		31-Dec-99		600	0	PROD
0015	408110008		TERMINAL DOUBLE TURRET										
			CONN	P 1 B P	EA	4	27-Jan-87		31-Dec-99		600	0	PROD
0076	430830003		RELAY REED 2FORMC DPDT										
			RELA	P 1 B P	EA	2	10-Sep-87		31-Dec-99		600	0	PROD
			K1,K2										
0081	433220002		FUSE PICO II 125V 3 AMP										
			FUSE	P 1 B P	EA	1	15-Jul-87		31-Dec-99		600	0	PROD
			F1										
0080	433221004		FUSE PICO II 125V 1 AMP										
			FUSE	P 1 B P	EA	3	15-Jul-87		31-Dec-99		600	0	PROD
			F2,F3,F4										
0082	454313003		HDR SOLD TAIL/MALE 3										
			CONN	P 1 B P	EA	2	15-Jul-87		31-Dec-99		600	0	PROD
			J3,J4										
0017	454313004		HDR SOLD TAIL/MALE 4										
			CONN	P 1 B P	EA	4	16-Dec-87		31-Dec-99		600	0	PROD
			J5										
0083	454370002		SHUNT 2 POS										
			SOCK	P 1 B P	EA	3	15-Jul-87		31-Dec-99		600	0	PROD
			P1,P2,P3										
0049	719100003		PC BD PREASS'Y 9100-3										
		4	PCB	P 1 B P	EA	1	01-Jan-70		31-Dec-99		600	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-4 BACKPLANE UM: EA PC: 4 ECN: 1006 ASSEMBLY QTY: 1
ERC: K SRCE CODE: A TYPE: 5 ABC: B PL: P DATE: 12-Jul-89

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0024	300060001	4	BEAD SHIELDING LARGE INDU	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0025	455011002		CONTACT (CRIMP) MALE CONN	P 1 B P EA	3	02-Oct-87		31-Dec-99		100	0	PROD
0015	455020004	4	CONTACT (CRIMP) FEMALE CONN	P 1 B P EA	17	24-Sep-87		31-Dec-99		100	0	PROD
0026	455110003		BLOCK FOR MALE PINS 3 CONN	P 1 B P EA	1	02-Oct-87		31-Dec-99		100	0	PROD
0014	455120018	4	BLOCK FOR FEM PINS 18 CONN	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0017	590001018		WIRE TEFLON 19/30 BLK 18 WIRE	P 1 B P EA	3	24-Sep-87		31-Dec-99		100	0	PROD
0022	590001022		WIRE TEFLON 7/30 BLK 22 WIRE	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0030	590221018		WIRE TEFLON 19/30 RED 18 WIRE	P 1 B P EA	0.550000	10-Jul-89		31-Dec-99		100	0	PROD
0031	590221022		WIRE TEFLON 7/30 RED 22 WIRE	P 1 B P EA	0.420000	10-Jul-89		31-Dec-99		100	0	PROD
0018	590221028		WIRE TEFLON 7/36 RED 28 WIRE	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0016	590331018		WIRE TEFLON 19/30 ORA 18 WIRE	P 1 B P EA	2	24-Sep-87		31-Dec-99		100	0	PROD
0021	590331022		WIRE TEFLON 7/30 ORA 22 WIRE	P 1 B P EA	2	24-Sep-87		31-Dec-99		100	0	PROD
0023	590441022		WIRE TEFLON 7/30 YEL 22 WIRE	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0020	590661018		WIRE TEFLON 19/30 BLU 18 WIRE	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0019	590771018		WIRE TEFLON 19/30 VIO 18 WIRE	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0032	594120001		TIEWRAP WIRE	P 1 B P EA	2	10-Jul-89		31-Dec-99		100	0	PROD
0013	719100004	4	PC BD W/CONN'S 9100-4 PCB	P 1 B P EA	1	01-Jan-70		31-Dec-99		100	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-5 DIP SW.BD. UM: EA PC: 4 ECN: 1001 ASSEMBLY QTY: 1
ERC: D SRCE CODE: A TYPE: 5 ABC: C PL: P DATE: 08-Apr-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0004	403950002		POLARIZING KEY															
				SOCK	P	1		B	P	EA	4	24-Sep-87		31-Dec-99		100	0	PROD
0001	411830001		SWITCH ROCKER PC MTG (8)															
				SWIT	P	1		B	P	EA	2	01-Jan-70		31-Dec-99		100	0	PROD
0002	454210020		HDR SOLD TAIL/MALE 20															
		4		CONN	P	1		B	P	EA	2	01-Jan-70		31-Dec-99		100	0	PROD
0087	510160001		GROUND LUG SPADE TYPE															
				HDWR	P	1		B	P	EA	4	25-Apr-90		31-Dec-99		100	0	PROD
			T1-T4															
0003	719100005		PC BD PREASS'Y 9100-5															
		4		PCB	P	1		B	P	EA	1	01-Jan-70		31-Dec-99		100	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6

TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0139	102412270		CAP CERA DISC 100V 27 PF										
			CAP	C56	P 1 B P EA	1	22-Oct-87		31-Dec-99		100	0	PROD
0009	103326473		CAP CERA MONO 50V .047UF										
			CAP	C6,C12,C13,C66	P 1 B P EA	4	28-Jun-90		31-Dec-99		100	0	PROD
0007	103336474		CAP CERA MONO 50V .47 UF										
			CAP	C14,C16,C17	P 1 B P EA	3	01-Jan-70		31-Dec-99		100	0	PROD
0017	106415102		CAP CERA MONO 100V .001UF										
		4	CAP	C9,C47,C62-C65	P 1 B P EA	6	25-Apr-90		31-Dec-99		100	0	PROD
0003	106415103		CAP CERA MONO 100V .01UF										
		4	CAP	C26,C102,C106,C108, C109,C118,C119,C121, C123,C130,C136,C140, C141,C153,C187,C200, C202,C208,C215,C225, C254,C255	P 1 B P EA	22	28-Jun-90		31-Dec-99		100	0	PROD
0137	106423018		CAP CERA MONO REEL 1.8PF										
		4	CAP	C55	P 1 B P EA	1	15-Jun-90		31-Dec-99		100	0	PROD
0138	106423056		CAP CERA MONO REEL 5.6PF										
		4	CAP	C54	P 1 B P EA	1	15-Jun-90		31-Dec-99		100	0	PROD
0002	106423120		CAP CERA MONO REEL 12PF										
		4	CAP	C25 [illegible] 67,C72,C73	P 1 B P EA	5	24-Apr-90		31-Dec-99		100	0	PROD
0004	106423390		CAP CERA MONO REEL 39PF										
		4	CAP	C10,C57,C58,C31,C34, C99	P 1 B P EA	6	24-Apr-90		31-Dec-99		100	0	PROD
0023	106425102		CAP CERA MONO REEL .001										
		4	CAP	C40-C42	P 1 B P EA	3	24-Apr-90		31-Dec-99		100	0	PROD
0006	106425103		CAP CERA MONO REEL .01UF										
			CAP	C100,C101,C103-C105 C107,C110,C111,C114, C117,C120,C122,C124- C127,C129,C131-C135, C137-C139,C142,C144- C152,C154-C170,C172- C186,C188-C199,C201, C203-C207,C209-C214, C216-C224,C226-C233, C235-C253,C256-C258, C260	P 1 B P EA	130	24-Apr-90		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / CODE / COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0008	106428104		CAP CERA MONO REEL .1UF									
		4	CAP	P 1 B P EA	18	24-Apr-90		31-Dec-99		100	0	PROD
			C1-C3,C7-C8,C22,C24, C27,C28,C30,C32,C36, C43,C45,C49,C69-C71									
0191	141268476		CAP TANT DIP CASE 10V 47UF									
		4	CAP	P 1 D P EA	3	24-Apr-90		31-Dec-99		100	0	PROD
			C19,C37,C44									
0141	141838335		CAP TANT DIP REEL 3.3UF									
			CAP	P 1 B P EA	8	24-Apr-90		31-Dec-99		100	0	PROD
			C4,C5,C15,C20,C38, C48,C39,C50									
0010	142824685		CAP TANT DIP CASE 6.8 UF									
			CAP	P 1 A P EA	3	04-Oct-88		31-Dec-99		100	0	PROD
			C51-C53									
0195	142864476		CAP TANT DIP CASE 47 UF									
		4	CAP	P 1 B P EA	2	14-Oct-88		31-Dec-99		100	0	PROD
			C18,C35									
0203	158819003		CAP VARIABLE 1.8 - 5 PF									
			CAP	P 1 B P EA	1	30-Mar-89		31-Dec-99		100	0	PROD
			C11									
0016	161225100		RES CARBON FILM 10 OHMS									
			RES	P 1 B P EA	3	23-Oct-87		31-Dec-99		100	0	PROD
			R120,R121,R122									
0012	161225101		RES CARBON FILM 100 OHMS									
			RES	P 1 B P EA	8	29-Jul-88		31-Dec-99		100	0	PROD
			R29,R30,R62,R129, R181,R183,R184,R189									
0013	161225102		RES CARBON FILM 1 K									
			RES	P 1 B P EA	10	04-Oct-88		31-Dec-99		100	0	PROD
			R52,R59,R60,R94,R114 R116,R117,R139,R185 R190									
0028	161225104		RES CARBON FILM 100 K									
			RES	P 1 B P EA	3	04-Oct-88		31-Dec-99		100	0	PROD
			R53,R149,R165									
0208	161225181		RES CARBON FILM 180 OHMS									
			RES	P 1 B P EA	7	15-Jun-89		31-Dec-99		100	0	PROD
			R142,R145,R146,R153, R155-R157									
0181	161225183		RES CARBON FILM 18 K									
			RES	P 1 B P EA	4	29-Jul-88		31-Dec-99		100	0	PROD
			R4,R15,R48,R68									
0033	161225221		RES CARBON FILM 220 OHMS									
			RES	P 1 B P EA	9	16-Mar-87		31-Dec-99		100	0	PROD
			R50,R51,R141,R143, R144,R147,R148,R150, R151									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0186	161225240		RES CARBON FILM 24 OHMS															
				RES		P	1		B	P	EA	1	29-Jul-88		31-Dec-99		100	0 PROD
				R180														
0031	161225272		RES CARBON FILM 2.7 K															
				RES		P	1		B	P	EA	27	04-Oct-88		31-Dec-99		100	0 PROD
				R20,R21,R26,R33,R36,														
				R47,R49,R64,R72,R79,														
				R81,R82,R85,R86,R91,														
				R93,R96,R98,R100,														
				R101,R103,R106,R108,														
				R111,R119,R124,R128														
0019	161225333		RES CARBON FILM 33 K															
				RES		P	1		B	P	EA	1	04-Oct-88		31-Dec-99		100	0 PROD
				R27														
0220	161225391		RES CARBON FILM 390 OHMS															
				RES		P	1		B	P	EA	2	12-May-89		31-Dec-99		100	0 PROD
				R38,R138														
0143	161225471		RES CARBON FILM 470 OHMS															
				RES		P	1		B	P	EA	6	04-Oct-88		31-Dec-99		100	0 PROD
				R42,R44,R63,R140,														
				R170,R171														
0061	161225510		RES CARBON FILM 51 OHMS															
				RES		P	1		B	P	EA	6	23-Oct-87		31-Dec-99		100	0 PROD
				R24,R25,R152,R154,														
				R166,R182														
0036	161225752		RES CARBON FILM 7.5 K															
				RES		P	1		B	P	EA	25	04-Oct-88		31-Dec-99		100	0 PROD
				R19,R22,R24,R34,R35,														
				R65,R73,R78,R80,R83,														
				R84,R87,R89,R92,R95,														
				R97,R99,R102,R104,														
				R107,R109,R110,R118														
				R123,R127														
0171	161335431		RES CARBON FILM 430 OHMS															
				RES		P	1		B	P	EA	1	03-Feb-88		31-Dec-99		100	0 PROD
				R232														
0154	161335470		RES CARBON FILM 47 OHMS															
				RES		P	1		B	P	EA	3	18-Nov-87		31-Dec-99		100	0 PROD
				R112,R113,R115														
0146	161445391		RES CARBON FILM 390 OHMS															
		4		RES		P	1		B	P	EA	2	23-Oct-87		31-Dec-99		100	0 PROD
				R76,R77														
0145	161445510		RES CARBON FILM 51 OHMS															
				RES		P	1		B	P	EA	1	23-Oct-87		31-Dec-99		100	0 PROD
				R125														
0169	168531234		RES PREC RN55D 22.1 OHMS															
		4		RES		P	1		B	P	EA	2	28-Jan-88		31-Dec-99		100	0 PROD
				R40,R169														

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / CODE / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0170	168531255		RES PREC RN55D 36.5 OHMS														
		4	RES		P		B	P	EA	2	28-Jan-88		31-Dec-99		100	0	PROD
			R41,R168														
0158	168531297		RES PREC RN55D 100 OHMS														
			RES		P		B	P	EA	2	18-Nov-87		31-Dec-99		100	0	PROD
			R31,R32														
0043	168531343		RES PREC RN55D 301 OHMS														
			RES		P		B	P	EA	2	25-Apr-90		31-Dec-99		100	0	PROD
			R46,R131														
0159	168531361		RES PREC RN55D 464 OHMS														
			RES		P		B	P	EA	4	18-Nov-87		31-Dec-99		100	0	PROD
			R1,R5,R6,R12														
0183	168531431		RES PREC RN55D 2.49 K														
			RES		P		B	P	EA	5	29-Jul-88		31-Dec-99		100	0	PROD
			R45,R58,R67,R133, R187														
0093	168531460		RES PREC RN55D 4.99 K														
			RES		P		B	P	EA	2	15-Jul-87		31-Dec-99		100	0	PROD
			R3,R14														
0037	168531474		RES PREC RN55D 6.98 K														
			RES		P		B	P	EA	6	16-Mar-87		31-Dec-99		100	0	PROD
			R2,R7-R9,R11,R16														
0095	168531489		RES PREC RN55D 10.0 K														
			RES		P		B	P	EA	2	20-Jul-88		31-Dec-99		100	0	PROD
			R57,R66														
0175	168531535		RES PREC RN55D 30.1 K														
			RES		P		B	P	EA	1	25-Apr-90		31-Dec-99		100	0	PROD
			R186														
0114	180247104		RES VARI CERMET 100 K														
			RES		P		B	P	EA	4	04-Oct-88		31-Dec-99		100	0	PROD
			R10,R13,R43,R132														
0148	180247502		RES VARI CERMET 5 K														
			RES		P		B	P	EA	3	04-Oct-88		31-Dec-99		100	0	PROD
			R74,R75,R188														
0032	190642101		RESISTOR NETWORK 100 OHMS														
			RES		P		B	P	EA	29	04-Oct-88		31-Dec-99		100	0	PROD
			U3,U16,U21,U23,U25, U52,U56,U66,U68,U70, U72,U79,U85,U87,U89, U93,U97,U99,U101, U108,U110,U112,U114, U116,U118,U128,U133, U137,U145														
0034	190642221		RESISTOR NETWORK 220 OHMS														
			RES		P		B	P	EA	1	16-Mar-87		31-Dec-99		100	0	PROD
			U34														

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0035	190842101		RESISTOR NETWORK 100 OHMS RES U27,U74,U106,U125, U130,U141,U143,U148	P 1 B P EA	8	04-Oct-88		31-Dec-99		100	0	PROD
0039	200031049		IC D-TYP FLOP SN74LS74N IC U33,U102	P 1 B P EA	2	01-Jan-70		31-Dec-99		100	0	PROD
0041	200031073		IC 2-IN POS OR SN74LS32N IC U38,U122	P 1 B P EA	2	07-Oct-86		31-Dec-99		100	0	PROD
0042	200031086		IC 2-INPUT AND SN74LS08N IC U82,U119	P 1 B P EA	2	07-Oct-86		31-Dec-99		100	0	PROD
0046	200041032		IC 13-INPUT NAND SN74S133 IC U37	P 1 B P EA	1	17-Dec-86		31-Dec-99		100	0	PROD
0199	200041039		IC MONO/MULTIVIB N74LS221 IC U120	P 1 B P EA	1	17-Oct-88		31-Dec-99		100	0	PROD
0045	200041062		IC DEC/DEMULTP SN74LS138N IC U49,U64	P 1 B P EA	2	01-Jan-70		31-Dec-99		100	0	PROD
0097	200041071		IC FULL ADDER SN74LS283N IC U40	P 1 B P EA	1	05-Aug-86		31-Dec-99		100	0	PROD
0047	200071001		IC 8 X BUFFER SN74LS240 IC U50,U83	P 1 B P EA	2	05-Aug-86		31-Dec-99		100	0	PROD
0048	200071377		IC 8XFLOP W/ENABL 74LS377 IC U47,U48,U62,U63	P 1 B P EA	4	01-Jan-70		31-Dec-99		100	0	PROD
0117	200330004		IC FAST HEX INV 74F04 IC U29,U121	P 1 B P EA	2	17-Dec-86		31-Dec-99		100	0	PROD
0098	200330033		IC QUAD 2-IN NOR SN74LS33 IC U103	P 1 B P EA	1	05-Aug-86		31-Dec-99		100	0	PROD
0049	200330260		IC 5-IN NOR GATE 74LS260 IC U81	P 1 B P EA	1	01-Jan-70		31-Dec-99		100	0	PROD
0161	200340070		IC M/S D-TYPE FLOP 11C70 IC U115	P 1 A P EA	1	18-Nov-87		31-Dec-99		100	0	PROD
0099	200340210		IC 3-IN 3-OUT OR MC10H210 IC U75,U92	P 1 B P EA	2	07-Oct-86		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0051	200340211		IC 3-IN/3-OUT NOR 10H211									
			IC	P 1 B P EA	2	07-Oct-86		31-Dec-99		100	0	PROD
			U71,U73									
0044	200344101		IC QUAD OR/NOR 10H101P									
			IC	P 1 B P EA	1	07-Oct-86		31-Dec-99		100	0	PROD
			U84									
0052	200344102		IC QUAD 2-IN NOR 10H102									
			IC	P 1 B P EA	2	23-Oct-87		31-Dec-99		100	0	PROD
			U100,U129									
0053	200344103		IC QUAD 2-IN OR 10H103									
			IC	P 1 B P EA	7	23-Oct-87		31-Dec-99		100	0	PROD
			U2,U9,U28,U51,U69, U86,U136									
0054	200344104		IC QUAD 2-IN NAND 10H104									
			IC	P 1 B P EA	5	28-Jan-88		31-Dec-99		100	0	PROD
			U4,U127,U131,U144 U147									
0056	200344107		IC 3X 2-IN OR/NOR 10H107									
			IC	P 1 B P EA	1	01-Jan-70		31-Dec-99		100	0	PROD
			U14									
0057	200344131		IC DUAL D M-S FLOP 10H131									
			IC	P 1 A P EA	13	04-Oct-88		31-Dec-99		100	0	PROD
			U15,U53,U55,U67,U80 U90,U94,U98,U104 U105,U117,U126,U132									
0058	200440292		IC FREQ DIV/TIMER 74LS292									
			IC	P 1 A P EA	1	01-Jan-70		31-Dec-99		100	0	PROD
			U35									
0059	200440592		IC 8-BIT BINARY CTR LS592									
			IC	P 1 A P EA	6	01-Jan-70		31-Dec-99		100	0	PROD
			U44-U46,U59-U61									
0060	200446016		IC HEX COUNTER 10H016									
		4	IC	P 1 A P EA	4	04-Dec-89		31-Dec-99		100	0	PROD
			U22,U57,U58,U96 TO BE TESTED BEFORE INSTALLATION.									
0200	204042005		IC TYP D FL-FL MC10131P									
			IC	P 1 A P EA	1	17-Oct-88		31-Dec-99		100	0	PROD
			U146									
0062	204042007		IC QUAD TRANSL MC10124P									
			IC	P 1 A P EA	2	07-Oct-86		31-Dec-99		100	0	PROD
			U36,U76									
0063	204042008		IC QUAD TRANSL MC10125P									
			IC	P 1 A P EA	4	16-Mar-87		31-Dec-99		100	0	PROD
			U32,U78,U124,U134									
0064	204042012		IC 2-IN AND GATE MC10104P									
			IC	P 1 B P EA	1	01-Jan-70		31-Dec-99		100	0	PROD
			U140									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0065	204042016		IC 2-INPUT OR/NOR F10101P														
			IC	P	1		B	P	EA	1	01-Jan-70		31-Dec-99		100	0	PROD
			U142														
0066	205632164		IC 8-BIT SHIFT REG HC164														
		4	IC	P	1		B	P	EA	2	05-Aug-86		31-Dec-99		100	0	PROD
			U26,U43														
0118	205640141		IC SHIFT REGISTER 10H141														
			IC	P	1		B	P	EA	4	17-Dec-86		31-Dec-99		100	0	PROD
			U107,U109,U111,U113														
0150	207143037		IC LINE DRIVER F3037														
			IC	P	1		B	P	EA	1	23-Oct-87		31-Dec-99		100	0	PROD
			U123														
0184	207257628		IC QUAD 8-BIT DAC 7628J														
			IC	P	1		B	P	EA	1	29-Jul-88		31-Dec-99		100	0	PROD
			U39														
0068	207344164		IC 8-LINE MPLX 10H164														
			IC	P	1		B	P	EA	1	05-Aug-86		31-Dec-99		100	0	PROD
			U24														
0069	207470640		IC BUS TRANSCEIVER LS640														
			IC	P	1		B	P	EA	1	01-Jan-70		31-Dec-99		100	0	PROD
			U65														
0070	208031010		IC QUAD DIFF COMP LM339N														
			IC	P	1		B	P	EA	1	05-Aug-86		31-Dec-99		100	0	PROD
			U30														
0071	208031084		IC QUAD J-FET OP AMP 084														
			IC	P	1		B	P	EA	1	18-Jan-88		31-Dec-99		100	0	PROD
			U1														
0176	208110412		IC OP AMP J-FET LF412														
		4	IC	P	3		B	P	EA	3	04-Oct-88		31-Dec-99		100	0	PROD
			U41,U42,U138														
0105	208166012		IC VOLT REG +12 UA78L12AC														
			IC	P	1		B	P	EA	1	19-Feb-87		31-Dec-99		100	0	PROD
			VR2														
0126	208217005		IC VOLT REG +5V MC78L05AC														
		4	IC	P	1		B	P	EA	1	11-Jun-87		31-Dec-99		100	0	PROD
			VR3														
0103	208510317		IC ADJ +V REG 317LZ														
			IC	P	1		B	P	EA	2	15-Jul-87		31-Dec-99		100	0	PROD
			VR4,VR6														
0122	208590012		IC -12V LO PWR REG 79L12A														
			IC	P	1		B	P	EA	1	19-Feb-87		31-Dec-99		100	0	PROD
			VR1														
0072	208590337		IC VOLT REG NEG ADJ LM337														
			IC	P	1		B	P	EA	1	04-Oct-88		31-Dec-99		100	0	PROD
			VR8														
0104	208765000		IC FREQ SYNTH SP5000														
		4	IC	P	1		B	P	EA	1	05-Aug-86		31-Dec-99		100	0	PROD
			U11														

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0075	230110005		DIODE SWITCHING 1N4448														
			DIOD		P	1		B	P	EA	7	04-Oct-88		31-Dec-99		100	0 PROD
			CR13,CR18-CR23														
0020	232140719		DIODE ARRAY(8 DIODES)2719														
			DIOD		P	1		B	P	EA	1	25-Apr-90		31-Dec-99		100	0 PROD
			U152														
0151	253012811		DIODE SCHOTTKY HP2811														
		4	DIOD		P	1		D	P	EA	4	04-Jun-90		31-Dec-99		100	0 PROD
0076	254110405		DIODE EPICAP BB405B														
			DIOD		P	1		B	P	EA	3	01-Jan-70		31-Dec-99		100	0 PROD
			CR9-11														
0086	270130401		TRANSISTOR NPN A401														
			XIST		P	1		A	P	EA	4	07-Oct-86		31-Dec-99		100	0 PROD
			Q8-Q11														
0077	270170001		TRANSISTOR NPN 2N5770														
			XIST		P	1		B	P	EA	3	25-Feb-88		31-Dec-99		100	0 PROD
			Q1,Q4,Q5														
0078	275170002		TRANSISTOR PNP 2N5771														
			XIST		P	1		A	P	EA	2	01-Jan-70		31-Dec-99		100	0 PROD
			Q2,Q3														
0177	280190224		TRANS FET "N" MTP12N08														
			XIST		P	1		B	P	EA	1	25-Feb-88		31-Dec-99		100	0 PROD
			Q13														
0079	300050001		CHOKE FERRITE SINGLE LEAD														
			INDU		P	1		A	P	EA	4	05-Aug-86		31-Dec-99		100	0 PROD
			L5-L8														
0160	301016090		INDUCTOR MOLDED .09 UH														
			INDU		P	1		B	P	EA	1	18-Nov-87		31-Dec-99		100	0 PROD
			L2														
0165	301016150		INDUCTOR MOLDED .15 UH														
		4	INDU		P	1		B	P	EA	1	03-Dec-87		31-Dec-99		100	0 PROD
			L3														
0107	301016221		INDUCTOR MOLDED .22 UH														
			INDU		P	1		B	P	EA	1	23-Oct-87		31-Dec-99		100	0 PROD
			L1														
0204	310243004		CRYSTAL 4.000 MHZ														
		4	CRYS		P	1		A	P	EA	1	05-May-89		31-Dec-99		100	0 PROD
			Y1														
0205	380212181		FOIL COPPER ADHESIVE BACK														
			CABL		P	1		B	P	EA	0	11-May-89		31-Dec-99		100	0 PROD
0109	402610005		CONN CO-AX PC MTG SMB														
		4	CONN		P	1		A	P	EA	11	19-May-89		31-Dec-99		100	0 PROD
			J601-J604,J608-J614														
0085	403170026		HDR DBL ROW RT ANGL 26														
			CONN		P	1		B	P	EA	1	01-Jan-70		31-Dec-99		100	0 PROD
			J617														

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6 TIMEBASE BD UM: EA PC: 4 ECN: 1027 ASSEMBLY QTY: 1
ERC: BB SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / CODE / COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0119	403181002		HDR SINGL ROW STRAIGHT 2 CONN P4,P6,P7	P 1 B P EA	3	15-Jul-87		31-Dec-99		100	0	PROD
0120	403181003		HDR SINGL ROW 3 CONN P3,P8,P9	P 1 B P EA	3	19-Feb-87		31-Dec-99		100	0	PROD
0128	403950002		POLARIZING KEY SOCK	P 1 B P EA	2	11-Jun-87		31-Dec-99		100	0	PROD
0201	430542712	4	RELAY 2 FORM C DPDT RELA U10	P 1 A P EA	1	17-Oct-88		31-Dec-99		100	0	PROD
0089	433225001		FUSE PICO II 125V 5 AMP FUSE F6,F8	P 1 B P EA	2	01-Jan-70		31-Dec-99		100	0	PROD
0123	454370002		SHUNT 2 POS SOCK J4,J8,J9	P 1 B P EA	3	25-Feb-88		31-Dec-99		100	0	PROD
0188	500860302		INSULATOR FOR TO-220 DIOD	P 1 A P EA	1	29-Jul-88		31-Dec-99		100	0	PROD
0132	505070002		HEAT SINK FOR TO-220 HEAT HS1	P 1 B P EA	1	15-Jul-87		31-Dec-99		100	0	PROD
0134	505112016	4	HEAT SINK FOR DIP-16 HEAT HS2,HS3,HS4,HS5	P 1 B P EA	4	18-Jan-88		31-Dec-99		100	0	PROD
0088	510160001		GROUND LUG SPADE TYPE HDWR T1-T4 QTY OF 4 TO BE SUPP- LIED BY PYRO.	P 1 B P EA	0	25-Apr-90		31-Dec-99		100	0	PROD
0187	555462002		NUT SELF-CLINCHING 4-40 HDWR	P 1 B P EA	1	29-Jul-88		31-Dec-99		100	0	PROD
0190	560440006		SCREW PHILIPS 4-40X3/8 HDWR	P 1 B P EA	1	29-Jul-88		31-Dec-99		100	0	PROD
0189	574409005		WASHER SHOULDER NYLON #4 HDWR	P 1 B P EA	1	29-Jul-88		31-Dec-99		100	0	PROD
0180	593920002		CABLE CO-AXIAL RG 188 A/U CABL	P 1 B P EA	1	07-Mar-88		31-Dec-99		100	0	PROD
0092	719100006	4	PC BD PREASS'Y 9100-6 PCB	P 1 A P EA	1	01-Jan-70		31-Dec-99		100	0	FAB
0202	CH599043013		HEAT SINK EPOXY CHEM	P 1 B P EA	0	05-Dec-88		31-Dec-99		100	0	CHEMICAL
0163	HFF231	C 4	IC DUAL FLIP-FLOP HYB U88	A 1 B P EA	1	18-Nov-87		31-Dec-99		100	0	SSDSUB
0073	MVL407	B 1	MULTI-CH MONO DISC MONO U12	A 1 P B P EA	1	01-Jan-70		31-Dec-99		100	4	HEPSUB

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-6

TIMEBASE BD
ERC: BB SRCE CODE: A TYPE: 1 UM: EA PC: 4 ABC: A PL: P

ECN: 1027 ASSEMBLY QTY: 1
DATE: 26-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY	PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0149	SM200150102	4	IC 2-IN OR/NOR 100102	IC U6		P	1	B	P	EA	1		23-Oct-87		31-Dec-99		100	0	PROD

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-7 COMPLETED FRONT PNL BD UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: J SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 08-Apr-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD.	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0015	103427104		CAP CERA MONO 100V .1 UF CAP C2-C7	P 1 A P EA	6	19-Sep-86		31-Dec-99		100	0	PROD
0016	147214221		CAP ALUM METAL CAN 220 UF CAP C1	P 1 B P EA	1	24-Jul-86		31-Dec-99		100	0	PROD
0011	161225103		RES CARBON FILM 10 K RES R2	P 1 B P EA	1	07-Jan-87		31-Dec-99		100	0	PROD
0012	161225154		RES CARBON FILM 150 K RES R1	P 1 B P EA	1	24-Jul-86		31-Dec-99		100	0	PROD
0006	161225222		RES CARBON FILM 2.2 K RES R18	P 1 B P EA	1	07-Jan-87		31-Dec-99		100	0	PROD
0013	161225821		RES CARBON FILM 820 OHMS RES R3-R17	P 1 B P EA	15	07-Jan-87		31-Dec-99		100	0	PROD
0008	200031021		IC HEX INVERTER SN7405N IC U2,U3	P 1 B P EA	2	24-Jul-86		31-Dec-99		100	0	PROD
0009	200031030		IC D-TYP FLOP SN7474N IC U4	P 1 B P EA	1	24-Jul-86		31-Dec-99		100	0	PROD
0010	200041044		IC MULTIVIBR SN74LS123N IC U1	P 1 B P EA	1	24-Jul-86		31-Dec-99		100	0	PROD
0007	200071377		IC 8XFLOP W/ENABL 74LS377 IC U5,U6	P 1 B P EA	2	24-Jul-86		31-Dec-99		100	0	PROD
0002	256282026		DIODE RED LED DIOD CR1-CR15	P 1 B P EA	15	24-Jul-86		31-Dec-99		100	0	PROD
0017	403950002		POLARIZING KEY SOCK	P 1 B P EA	2	10-Jun-87		31-Dec-99		100	0	PROD
0004	416181001	4	SWITCH PUSHBUTTON SPST SWIT -	P 3 B P EA	2	06-Aug-86		31-Dec-99		100	0	PROD
0005	454610026		HDR SOLD TAIL/MALE 26 CONN P1	P 1 B P EA	1	25-Sep-86		31-Dec-99		100	0	PROD
0003	520600110	4	SPACER NYLON #6 .312 LG HDWR	P 1 B P EA	15	24-Jul-86		31-Dec-99		100	0	PROD
0001	719100007	4	PC BD PREASS'Y 9100-7 PCB	P 1 B P EA	1	24-Jul-86		31-Dec-99		100	0	FAB

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-7

COMPLETED FRONT PNL BD
ERC: J SRCE CODE: A TYPE: 1 UM: EA PC: 4 ABC: B PL: P

ECN: 1003 ASSEMBLY QTY: 1
DATE: 08-Apr-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR LT SEQ OFF	STORES ACCOUNT

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-8 CARD CAGE/PWR SUPPLY UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: U SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 17-Jan-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0035	300060001		BEAD SHIELDING LARGE									
		4	INDU	P 1 B P EA	1	12-Jul-89		31-Dec-99		100	0	PROD
0013	315070150		POWER SUPPLY 150W									
		4	PWRS	P 1 A P EA	1	20-Oct-89		31-Dec-99		100	0	FAB
0034	455011002		CONTACT (CRIMP) MALE									
			CONN	P 1 B P EA	3	12-Jul-89		31-Dec-99		100	0	PROD
0036	455020004		CONTACT (CRIMP) FEMALE									
		4	CONN	P 1 B P EA	17	12-Jul-89		31-Dec-99		100	0	PROD
0029	455021008		CONTACT (CRIMP) FEMALE									
			CONN	P 1 B P EA	1	07-Oct-87		31-Dec-99		100	0	PROD
0037	455110003		BLOCK FOR MALE PINS 3									
			CONN	P 1 B P EA	1	12-Jul-89		31-Dec-99		100	0	PROD
0038	455120018		BLOCK FOR FEM PINS 18									
		4	CONN	P 1 B P EA	1	12-Jul-89		31-Dec-99		100	0	PROD
0015	485023006		BUMPER (FOOT) BLK RUBBER									
		4	HDWR	P 1 B P EA	1	23-Sep-87		31-Dec-99		100	0	PROD
0011	530409503		CARD GUIDE 6.5" LONG									
			FAN	P 1 B P EA	12	13-Aug-86		31-Dec-99		100	0	PROD
0009	560440004		SCREW PHILIPS 4-40X1/4									
			HDWR	P 1 B P EA	13	23-Sep-87		31-Dec-99		100	0	PROD
0014	560440006		SCREW PHILIPS 4-40X3/8									
			HDWR	P 1 B P EA	1	17-Oct-88		31-Dec-99		100	0	PROD
0008	560632004		SCREW PHILIPS 6-32X1/4									
			HDWR	P 1 B P EA	10	04-Feb-88		31-Dec-99		100	0	PROD
0031	560632007		SCREW PHILIPS 6-32X7/16									
			HDWR	P 1 B P EA	2	11-Feb-88		31-Dec-99		100	0	PROD
0016	560832006		SCREW PHILIPS 8-32X3/8									
			HDWR	P 1 B P EA	4	23-Sep-87		31-Dec-99		100	0	PROD
0018	575810002		WASHER FLAT REG OD SIZE 8									
			HDWR	P 1 B P EA	4	23-Sep-87		31-Dec-99		100	0	PROD
0019	576410001		WASHER SPLIT LOCK SIZE 4									
			HDWR	P 1 B P EA	9	23-Sep-87		31-Dec-99		100	0	PROD
0017	576810001		WASHER SPLIT LOCK SIZE 8									
			HDWR	P 1 B P EA	4	23-Sep-87		31-Dec-99		100	0	PROD
0039	590001018		WIRE TEFLON 19/30 BLK 18									
			WIRE	P 1 B P EA	3	12-Jul-89		31-Dec-99		100	0	PROD
0040	590001022		WIRE TEFLON 7/30 BLK 22									
			WIRE	P 1 B P EA	1	12-Jul-89		31-Dec-99		100	0	PROD
0041	590221018		WIRE TEFLON 19/30 RED 18									
			WIRE	P 1 B P EA	0.550000	12-Jul-89		31-Dec-99		100	0	PROD
0042	590221022		WIRE TEFLON 7/30 RED 22									
			WIRE	P 1 B P EA	0.420000	12-Jul-89		31-Dec-99		100	0	PROD
0044	590331018		WIRE TEFLON 19/30 ORA 18									
			WIRE	P 1 B P EA	2	12-Jul-89		31-Dec-99		100	0	PROD
0025	590331022		WIRE TEFLON 7/30 ORA 22									
			WIRE	P 1 B P EA	2	24-Sep-87		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-8 CARD CAGE/PWR SUPPLY UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: U SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 17-Jan-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0046	590441022		WIRE TEFLON 7/30 YEL 22	WIRE	P	1		B	P	EA	1	12-Jul-89		31-Dec-99		100	0	PROD
0047	590661018		WIRE TEFLON 19/30 BLU 18	WIRE	P	1		B	P	EA	1	12-Jul-89		31-Dec-99		100	0	PROD
0048	590771018		WIRE TEFLON 19/30 VIO 18	WIRE	P	1		B	P	EA	1	12-Jul-89		31-Dec-99		100	0	PROD
0049	594120001		TIEWRAP	WIRE	P	1		B	P	EA	2	12-Jul-89		31-Dec-99		100	0	PROD
0030	595003102		SLEEVING SHRINK BLK 1/8"	WIRE	P	1		B	P	EA	1	07-Oct-87		31-Dec-99		100	0	PROD
0001	709100004	4	CHASSIS BASE PLATE	FAB	P	1		B	P	EA	1	05-Aug-86		31-Dec-99		100	0	FAB
0004	709100007	4	AIR DEFLECTION PLATE	FAB	P	1		B	P	EA	1	05-Aug-86		31-Dec-99		100	0	FAB
0005	709100008	4	CHASSIS SUPPORT CHANNEL	FAB	P	1		B	P	EA	2	05-Aug-86		31-Dec-99		100	0	FAB
0006	709100009	4	LOCK PLATE	FAB	P	1		B	P	EA	2	05-Aug-86		31-Dec-99		100	0	FAB
0032	709100035	B	MULTIBUS CHASSIS 9100	FAB	P	1		A	P	EA	2	17-Oct-88		31-Dec-99		100	0	FAB
0033	709100036	4	BAR (SUPPORT) 9100	FAB	P	1		B	P	EA	1	17-Oct-88		31-Dec-99		100	0	FAB
0051	719100017	4	PC BD PREASS'Y 9100-17	PCB	P	1		A	P	EA	1	06-Apr-90		31-Dec-99		100	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-9 FRONT PNL ASS'Y 9100-9 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: N SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 06-Jun-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0022	377080001		LABEL "PC BOARDS INTERCONNECT"														
		4	FAB	P	1		B	P	EA	1	02-Oct-87		31-Dec-99		100	0	FAB
0034	411271001		SWITCH ROCKER DPST														
		4	SWIT	P	1		B	P	EA	1	24-Mar-88		31-Dec-99		100	0	PROD
0021	455011002		CONTACT (CRIMP) MALE														
			CONN	P	1		B	P	EA	5	24-Sep-87		31-Dec-99		100	0	PROD
0019	455120006		BLOCK FOR MALE PINS 6														
		4	CONN	P	1		B	P	EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0035	555500003		SCREW TRUSS HD 4-40X3/4														
		4	HDWR	P	1		B	P	EA	4	10-Apr-89		31-Dec-99		100	0	PROD
0030	560440003		SCREW PHILIPS 4-40X3/16														
			HDWR	P	1		B	P	EA	2	06-Nov-87		31-Dec-99		100	0	PROD
0011	560440005		SCREW PHILIPS 4-40X5/16														
			HDWR	P	1		B	P	EA	6	07-Oct-87		31-Dec-99		100	0	PROD
0029	560440006		SCREW PHILIPS 4-40X3/8														
			HDWR	P	1		B	P	EA	2	03-Nov-87		31-Dec-99		100	0	PROD
0033	575410012		WASHER FLAT (THIN) #4														
			HDWR	P	3		B	P	EA	16	01-Dec-87		31-Dec-99		100	0	PROD
0024	576410001		WASHER SPLIT LOCK SIZE 4														
			HDWR	P	1		B	P	EA	18	01-Dec-87		31-Dec-99		100	0	PROD
0012	580440001		NUT HEX STANDARD 4-40														
			HDWR	P	1		B	P	EA	13	01-Dec-87		31-Dec-99		100	0	PROD
0031	581440001		NUT HEX SMALL OD SIZE 4														
			HDWR	P	1		B	P	EA	2	01-Dec-87		31-Dec-99		100	0	PROD
0028	589904226		CABLE SHIELDED 4-COND														
		4	CABL	P	1		B	P	EA	1	28-Oct-87		31-Dec-99		100	0	PROD
0018	590001018		WIRE TEFLON 19/30 BLK 18														
			WIRE	P	1		B	P	EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0017	590091018		WIRE TEFLON 19/30 BLK/WHT 18														
			WIRE	P	1		B	P	EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0014	590331022		WIRE TEFLON 7/30 ORA 22														
			WIRE	P	1		B	P	EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0015	590941018		WIRE TEFLON 19/30 WHT/YEL 18														
			WIRE	P	1		B	P	EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0016	590991018		WIRE TEFLON 19/30 WHT 18														
			WIRE	P	1		B	P	EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0006	594120004		CABLE TIE WITH SCREW BASE														
		4	CABL	P	3		B	P	EA	3	01-Dec-87		31-Dec-99		100	0	PROD
0027	595003102		SLEEVING SHRINK BLK 1/8"														
			WIRE	P	1		B	P	EA	1	07-Oct-87		31-Dec-99		100	0	PROD
0008	709100002		FRONT PANEL														
		4	FAB	P	1		B	P	EA	1	06-Aug-86		31-Dec-99		100	0	FAB
0036	709100014		BRACKET FOR BOBBIN ("U") 9100														
			FAB	P	1		B	P	EA	2	12-Jul-89		31-Dec-99		100	0	FAB
0037	709100015		BRACKET FOR BOBBIN 9100														
			FAB	P	1		B	P	EA	2	12-Jul-89		31-Dec-99		100	0	FAB

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-9 FRONT PNL ASS'Y 9100-9 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: N SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 06-Jun-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0025	709100024		PC BOARD SUPPORT														
		4	FAB	P	1		B	P	EA	1	07-Oct-87		31-Dec-99		100	0	FAB
0026	709100025		BRACKET PC SUPPORT 9100														
		4	FAB	P	1		B	P	EA	2	15-Aug-89		31-Dec-99		100	0	FAB
0032	709109002		FRONT PNL BRACKET 9109														
		4	FAB	P	1		B	P	EA	4	06-Jun-90		31-Dec-99		100	0	FAB
0001	9100-7	J	COMPLETED FRONT PNL BD														
		4	ASSY	A	1		B	P	EA	1	30-Jul-86		31-Dec-99		600	0	SSDSUB
0038	9100-H1	B	CABLE CO-AX 10" BNC/SMB														
		4	FAB	P	1		A	P	EA	4	12-Jul-89		31-Dec-99		100	0	FAB
0039	9100-H13	B	CABLE (19NS DELAY)SMB-SMB														
		4	FAB	P	1		A	P	EA	1	12-Jul-89		31-Dec-99		100	0	FAB
0040	9100-H14	B	CABLE (19.5NS DELAY) SMB-SMB														
		4	FAB	P	1		A	P	EA	1	12-Jul-89		31-Dec-99		100	0	FAB
0041	9100-H15	B	RIBBON CABLE 1" 34 COND														
		4	FAB	P	1		B	P	EA	2	12-Jul-89		31-Dec-99		100	0	FAB
0043	9100-H18	A	RIBBON CABLE 5" 26 COND														
		4	FAB	P	1		B	P	EA	1	12-Jul-89		31-Dec-99		100	0	FAB
0042	9100-H22	C	CABLE 14" 5 COND														
		4	FAB	P	1		A	P	EA	1	12-Jul-89		31-Dec-99		100	0	FAB
0044	9100-H5	B	CABLE CO-AX 16" BNC-SMB														
		4	FAB	P	1		A	P	EA	3	12-Jul-89		31-Dec-99		100	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-10 REAR PNL ASS'Y 9100-10 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: Y SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 27-Apr-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0053	195212003		VARISTOR 130V 20 JOULES RES	P 1 B P EA	1	02-Oct-87		31-Dec-99		100	0	PROD
0081	312605000	4	BATTERY LITH 3V "C" CELL BATT	P 1 B P EA	1	01-Jul-90		31-Dec-99		100	0	PROD
0059	315910003	4	LINE FILTER - RFI 3A INDU	P 1 B P EA	1	31-Mar-88		31-Dec-99		100	0	PROD
0054	377041043	4	LABEL "-1...OPTIONS" LABE	P 1 B P EA	1	20-Jul-89		31-Dec-99		100	0	PROD
0076	403950002		POLARIZING KEY SOCK	P 1 B P EA	4	12-Jul-89		31-Dec-99		100	0	PROD
0002	405354001		SCREWLOCK ASSY KIT FEMALE CONN	P 1 B P EA	1	13-Aug-86		31-Dec-99		100	0	PROD
0004	411472001		SWITCH ROCKER 2A250V 4PDT SWIT	P 1 B P EA	1	07-Aug-86		31-Dec-99		100	0	PROD
0077	411830001		SWITCH ROCKER PC MTG (8) SWIT	P 1 B P EA	2	12-Jul-89		31-Dec-99		100	0	PROD
0035	433112002	4	FUSE SLO-BLO 250V 1.5 AMP FUSE	P 1 B P EA	1	06-Jul-87		31-Dec-99		100	0	PROD
0055	433312003	4	FUSE FAST-BLO 3 AMP FUSE	P 1 B P EA	1	02-Oct-87		31-Dec-99		100	0	PROD
0058	434182001		FUSEHOLDER PANEL MTG FUSE	P 1 B P EA	2	05-Oct-87		31-Dec-99		100	0	PROD
0083	453211026	4	CONN FL CABL MALE 26 CONN	P 1 B P EA	1	01-Jul-90		31-Dec-99		100	0	PROD
0016	453910003		CONN HDW KIT METRIC CONN	P 1 B P EA	1	13-Aug-86		31-Dec-99		100	0	PROD
0078	454210020	4	HDR SOLD TAIL/MALE 20 CONN	P 1 B P EA	2	12-Jul-89		31-Dec-99		100	0	PROD
0052	454390009	4	TERMINAL STRIP ASSEMBLY CONN	P 1 A P EA	1	02-Oct-87		31-Dec-99		100	0	PROD
0047	455020004	4	CONTACT (CRIMP) FEMALE CONN	P 1 B P EA	6	24-Sep-87		31-Dec-99		100	0	PROD
0050	455021008		CONTACT (CRIMP) FEMALE CONN	P 1 B P EA	6	07-Oct-87		31-Dec-99		100	0	PROD
0051	455120003		BLOCK FOR FEM PINS 3 CONN	P 1 B P EA	1	02-Oct-87		31-Dec-99		100	0	PROD
0027	455123005		BLOCK FOR FEM PINS 5 CONN	P 1 B P EA	2	23-Sep-87		31-Dec-99		100	0	PROD
0046	455211006	4	BLOCK FOR FEM PINS 6 CONN	P 1 B P EA	1	24-Sep-87		31-Dec-99		100	0	PROD
0082	515404001	4	BATTERY HOLDER "C" CELL BATT	P 1 B P EA	2	01-Jul-90		31-Dec-99		100	0	PROD
0057	522632024	4	SPACER ROUND 6-32X3/4 HDWR	P 1 B P EA	2	05-Oct-87		31-Dec-99		100	0	PROD
0014	530409106		FAN AXIAL 50-60 HZ 115V FAN	P 1 A P EA	2	13-Aug-86		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-10 REAR PNL ASS'Y 9100-10 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: Y SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 27-Apr-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0015	530409994		FAN FILTER W/FOAM PAD														
		4	FAN	P	1		B	P	EA	2	13-Aug-86		31-Dec-99		100	0	PROD
0007	560440003		SCREW PHILIPS 4-40X3/16														
			HDWR	P	1		B	P	EA	4	28-Oct-86		31-Dec-99		100	0	PROD
0056	560632004		SCREW PHILIPS 6-32X1/4														
			HDWR	P	1		B	P	EA	2	02-Oct-87		31-Dec-99		100	0	PROD
0084	567440008		SCREW FLAT PHIL 4-40X1/2														
			HDWR	P	1		B	P	EA	2	01-Jul-90		31-Dec-99		100	0	PROD
0006	567632012		SCREW FLAT PHIL 6-32X3/4														
		4	HDWR	P	1		B	P	EA	8	07-Aug-86		31-Dec-99		100	0	PROD
0022	575410012		WASHER FLAT (THIN) #4														
			HDWR	P	3		B	P	EA	8	28-Oct-86		31-Dec-99		100	0	PROD
0037	576010001		WASHER SPLIT LOCK SIZE 10														
			HDWR	P	1		B	P	EA	2	10-Sep-87		31-Dec-99		100	0	PROD
0019	576410001		WASHER SPLIT LOCK SIZE 4														
			HDWR	P	1		B	P	EA	6	20-Oct-86		31-Dec-99		100	0	PROD
0018	577600001		WASHER SHAKEPROOF SIZE 6														
			HDWR	P	1		B	P	EA	8	20-Oct-86		31-Dec-99		100	0	PROD
0017	580440001		NUT HEX STANDARD 4-40														
			HDWR	P	1		B	P	EA	6	20-Oct-86		31-Dec-99		100	0	PROD
0060	580632002		NUT HEX														
		4	HDWR	P	1		B	P	EA	8	26-Apr-88		31-Dec-99		100	0	PROD
0028	590001018		WIRE TEFLON 19/30 BLK 18														
			WIRE	P	1		B	P	EA	7.040000	21-Oct-86		31-Dec-99		100	0	PROD
0064	590001022		WIRE TEFLON 7/30 BLK 22														
			WIRE	P	1		B	P	EA	1.340000	16-May-89		31-Dec-99		100	0	PROD
0048	590091018		WIRE TEFLON 19/30 BLK/WHT 18														
			WIRE	P	1		B	P	EA	1.590000	24-Sep-87		31-Dec-99		100	0	PROD
0063	590221022		WIRE TEFLON 7/30 RED 22														
			WIRE	P	1		B	P	EA	1.340000	16-May-89		31-Dec-99		100	0	PROD
0030	590331018		WIRE TEFLON 19/30 ORA 18														
			WIRE	P	1		B	P	EA	1.250000	21-Oct-86		31-Dec-99		100	0	PROD
0031	590441018		WIRE TEFLON 19/30 YEL 18														
			WIRE	P	1		B	P	EA	0.750000	21-Oct-86		31-Dec-99		100	0	PROD
0032	590551018		WIRE TEFLON 19/30 GRN 18														
			WIRE	P	1		B	P	EA	2.800000	21-Oct-86		31-Dec-99		100	0	PROD
0029	590661018		WIRE TEFLON 19/30 BLU 18														
			WIRE	P	1		B	P	EA	0.750000	21-Oct-86		31-Dec-99		100	0	PROD
0049	590941018		WIRE TEFLON 19/30 WHT/YEL 18														
			WIRE	P	1		B	P	EA	1.630000	24-Sep-87		31-Dec-99		100	0	PROD
0033	590991018		WIRE TEFLON 19/30 WHT 18														
			WIRE	P	1		B	P	EA	2.750000	21-Oct-86		31-Dec-99		100	0	PROD
0065	590991022		WIRE TEFLON 7/30 WHT 22														
			WIRE	P	1		B	P	EA	1.170000	16-May-89		31-Dec-99		100	0	PROD
0066	594120001		TIEWRAP														
			WIRE	P	1		B	P	EA	7	16-May-89		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-10 REAR PNL ASS'Y 9100-10 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: Y SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 27-Apr-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0069	595003104		SLEEVING SHRINK BLK 3/8"														
			WIRE		P	1		B	P EA	0.500000	31-May-89		31-Dec-99		100	0	PROD
0068	595031105		SLEEVING SHRINK BLK 3/16"														
			WIRE		P	1		B	P EA	1.250000	31-May-89		31-Dec-99		100	0	PROD
0080	595901014		SLEEVING TEFLON AWG 14														
		4	WIRE		P	1		B	P EA	0.100000	13-Sep-89		31-Dec-99		100	0	PROD
0036	709100012		HOLE PLUG (BLK)														
		4	FAB		P	1		B	P EA	7	05-Dec-86		31-Dec-99		100	0	FAB
0085	709100038		BACK PANEL														
		4	FAB		P	1		A	P EA	1	01-Jul-90		31-Dec-99		100	0	FAB
0079	719100005		PC BD PREASS'Y 9100-5														
		4	PCB		P	1		B	P EA	1	12-Jul-89		31-Dec-99		100	0	FAB
0070	9100-H12	B	CABLE CO-AX 3" SMB-SMB														
		4	FAB		P	1		A	P EA	1	12-Jul-89		31-Dec-99		300	0	FAB
0072	9100-H17	C	RIBBON CABLE 1" 26 COND														
		4	FAB		P	1		B	P EA	1	12-Jul-89		31-Dec-99		300	0	FAB
0071	9100-H19	A	RIBBON CABLE 19" 26 COND														
		4	FAB		P	1		A	P EA	1	12-Jul-89		31-Dec-99		100	0	FAB
0073	9100-H20	B	RIBBON CABLE 19" 26 COND														
		4	FAB		P	1		A	P EA	1	12-Jul-89		31-Dec-99		100	0	FAB
0074	9100-H21	A	RIBBON CABLE ASS'Y (2) 20 COND														
		4	FAB		P	1		A	P EA	1	12-Jul-89		31-Dec-99		300	0	FAB
0075	9100-H8	C	CABLE CO-AX 21" BNC-SMB														
		4	FAB		P	1		A	P EA	4	12-Jul-89		31-Dec-99		100	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-13 BOARD 186/03A CPU 9100-13 UM: EA PC: 4 ECN: 1014 ASSEMBLY QTY: 1
ERC: O SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 22-Nov-88

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0007	161335102		RES CARBON FILM 1 K															
				RES	P	1		B	P	EA	1	22-Nov-88		31-Dec-99		100	0	PROD
0001	200906186		SINGLE BOARD COMPUTER 186/03A															
		4		IC	P	1		B	P	EA	1	06-Apr-87		31-Dec-99		100	0	PROD
0003	205270264		IC 8192X8 RAM 6264LP-12															
				IC	P	1		A	P	EA	4	06-Apr-87		31-Dec-99		100	0	PROD
0002	205370512		IC 65536X8 UV PROM 27512															
				IC	P	1		A	P	EA	4	06-Apr-87		31-Dec-99		100	0	PROD
			NOTE; DO NOT INCLUDE ON KIT. GIVE TO PROGRAMMING CENTER, EXCEPT FOR, 9100 SERIES GOES TO S.S.D. TEST															
0005	403950002		POLARIZING KEY															
				SOCK	P	1		B	P	EA	6	10-Jun-87		31-Dec-99		100	0	PROD
0004	403980002		SHUNT ASSEMBLY 2-POS															
				SOCK	P	1		B	P	EA	11	11-May-88		31-Dec-99		100	0	PROD
0006	528055014		PLUG(POTTING BASE) DIP-14															
				PROD	P	1		B	P	EA	1	22-Oct-87		31-Dec-99		100	0	PROD

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-16

COMPLETED BOARD 9100-16 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: P SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 06-Aug-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0001	102412220		CAP CERA DISC 100V 22 PF CAP C8,C9			P	B	1	EA	2	11-Oct-88		31-Dec-99		100	0	PROD
0003	103437104		CAP CERA MONO 100V .1 UF CAP C58			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0004	106415103	4	CAP CERA MONO 100V .01UF CAP C1,C2,C4-C7,C11-C27, C30-C33,C39-C47,C49, C50,C51,C53-C57,C59- C69,C71-C73,C76			P	B	1	EA	59	28-Jun-90		31-Dec-99		100	0	PROD
0071	142124476		CAP TANT DIP CASE 47 UF CAP C77			P	B	1	EA	1	30-Aug-89		31-Dec-99		100	0	PROD
0006	146424106		CAP MINI ALUM 20% 10 UF CAP C3,C10,C28,C29,C34, C35-C38,C48,C52,C70 C75			P	B	1	EA	13	01-Feb-89		31-Dec-99		100	0	PROD
0007	161225101		RES CARBON FILM 100 OHMS RES R5,R6			P	B	1	EA	2	23-May-90		31-Dec-99		100	0	PROD
0168	161225102		RES CARBON FILM 1 K RES R3			P	B	1	EA	1	01-Feb-89		31-Dec-99		100	0	PROD
0008	161225103		RES CARBON FILM 10 K RES R1,R7,R12			P	B	1	EA	3	21-Oct-88		31-Dec-99		100	0	PROD
0009	161225222		RES CARBON FILM 2.2 K RES R4			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0069	161225471		RES CARBON FILM 470 OHMS RES R2			P	B	1	EA	1	23-May-90		31-Dec-99		100	0	PROD
0062	161335185		RES CARBON FILM 1.8 MEG RES R9			P	B	3	EA	1	20-Dec-88		31-Dec-99		100	0	PROD
0063	168531509		RES PREC RN55D 16.2 K RES R11			P	B	1	EA	1	20-Dec-88		31-Dec-99		100	0	PROD
0064	168531545		RES PREC RN55D 38.3 K RES R10			P	B	1	EA	1	20-Dec-88		31-Dec-99		100	0	PROD
0065	168531553		RES PREC RN55D 46.4 K RES R8			P	B	1	EA	1	20-Dec-88		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-16 COMPLETED BOARD 9100-16 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: P SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 06-Aug-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0010	190042102		RESISTOR NETWORK 1 K									
			RES	P 1 B P EA	2	11-Oct-88		31-Dec-99		100	0	PROD
			U60,U73									
0011	190042222		RESISTOR NETWORK 2.2 K									
			RES	P 1 B P EA	7	01-Feb-89		31-Dec-99		100	0	PROD
			U14,U16,U26,U32,U35, U41,U47									
0012	190642102		RESISTOR NETWORK 1 K									
			RES	P 1 B P EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			U10									
0013	200031046		IC HEX INVERTER SN74LS04N									
			IC	P 1 B P EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			U6									
0014	200031049		IC D-TYP FLOP SN74LS74N									
			IC	P 1 B P EA	2	11-Oct-88		31-Dec-99		100	0	PROD
			U1,U18									
0015	200031073		IC 2-IN POS OR SN74LS32N									
			IC	P 1 B P EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			U2									
0016	200031086		IC 2-INPUT AND SN74LS08N									
			IC	P 1 B P EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			U11									
0017	200041062		IC DEC/DEMULTP SN74LS138N									
			IC	P 1 B P EA	2	11-Oct-88		31-Dec-99		100	0	PROD
			U36,U38									
0018	200071001		IC 8 X BUFFER SN74LS240									
			IC	P 1 B P EA	4	11-Oct-88		31-Dec-99		100	0	PROD
			U15,U25,U27,U31									
0019	200071005		IC D-TYP FLOP SN74LS273N									
			IC	P 1 B P EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			U7									
0020	200071007		IC BUFFER SN74LS244N									
			IC	P 1 B P EA	2	11-Oct-88		31-Dec-99		100	0	PROD
			U8,U17									
0021	200071245		IC BUS XCEIVER SN74LS245N									
			IC	P 1 B P EA	2	11-Oct-88		31-Dec-99		100	0	PROD
			U23,U24									
0022	200071373		IC D-TYP LATCH 74LS373N									
			IC	P 1 B P EA	3	11-Oct-88		31-Dec-99		100	0	PROD
			U4,U19,U20									
0023	200344138		IC 3-TO-8 DECODER 138									
			IC	P 1 B P EA	2	11-Oct-88		31-Dec-99		100	0	PROD
			U66,U69									
0024	205271256		IC 32K X 8 RAM 62256-12									
			IC	P 1 A P EA	18	11-Oct-88		31-Dec-99		100	0	PROD
			U39,U40,U44,U45,U49, U50,U53-U56,U58,U59, U62,U63,U67,U68,U70, U71									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-16 COMPLETED BOARD 9100-16 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: P SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 06-Aug-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0025	205370512		IC 65536X8 UV PROM 27512 IC U28,U29,U33,U34 GIVE TO SSD MANU.			P	A	1	EA	4	11-Oct-88		31-Dec-99		300	0	PROD
0026	205750168		IC 7-WIDE AND-OR-INV 16L8 IC U3,U12,U22 GIVE TO SSD MANU.			P	B	1	EA	3	11-Oct-88		31-Dec-99		300	0	PROD
0028	207170540		IC BUFF/LINE DRIV 74LS540 IC U9,U61,U74			P	B	1	EA	3	11-Oct-88		31-Dec-99		100	0	PROD
0052	207440232		IC XMTR/RCVR MAX232 IC U43			P	B	1	EA	1	21-Oct-88		31-Dec-99		100	0	PROD
0030	207470160		IC BUS TRANSCEIVER 75160B IC U48			P	A	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0031	207470640		IC BUS TRANSCEIVER LS640 IC U37,U42,U46			P	B	1	EA	3	11-Oct-88		31-Dec-99		100	0	PROD
0032	207490162		IC OCTAL BUS XCVR 75162A IC U52			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0066	208031010		IC QUAD DIFF COMP LM339N IC U72			P	B	1	EA	1	20-Dec-88		31-Dec-99		100	0	PROD
0033	208517705		IC VOLTAGE REG 7705 IC U64			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0051	227024254	4	IC INTERVAL TIMER 8254 IC U30			P	B	1	EA	1	21-Oct-88		31-Dec-99		100	0	PROD
0036	227028259	4	IC INTERRUPT CONTROLLER 8259A IC U21			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0037	227040274	4	IC MPSC 8274 IC U65			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0038	227120288	4	IC BUS CONTROLLER 8288 IC U51			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0039	227799914		IC GPIB CONTROL TMS9914A IC U57			P	A	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
0041	240425746		DIODE ZENER 3.3V 1N746A DIOD CR1			P	B	1	EA	1	11-Oct-88		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-16 COMPLETED BOARD 9100-16 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: P SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 06-Aug-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0053	253050817		DIODE HOT CARRIER 1N5817														
			DIOD		P	1	B	P	EA	2	01-Feb-89		31-Dec-99		100	0	PROD
			CR2,CR3														
0042	270110003		TRANSISTOR NPN PN2222A														
			XIST		P	1	B	P	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			Q1														
0043	300050001		CHOKE FERRITE SINGLE LEAD														
			INDU		P	1	A	P	EA	2	11-Oct-88		31-Dec-99		100	0	PROD
			L1,L2														
0044	310060157		CRYSTAL 15.75 MHZ														
		4	CRYS		P	1	B	P	EA	1	02-Aug-89		31-Dec-99		100	0	PROD
0054	400062228		SOCKET IC AUTO INSERTION DIP 28														
		4	SOCK		P	1	*	P	EA	4	06-Aug-90		31-Dec-99		100	0	PROD
0055	400071020		SOCKET IC SOLD TAIL DIP-20														
			SOCK		P	1	B	P	EA	3	07-Nov-88		31-Dec-99		100	0	PROD
0045	400418068		IC SOCKET GRID TYPE 68-PIN														
		4	SOCK		P	1	B	P	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			U13														
0046	403170026		HDR DBL ROW RT ANGL 26														
			CONN		P	1	B	P	EA	3	11-Oct-88		31-Dec-99		100	0	PROD
			J2,J4,J5														
0072	403181003		HDR SINGL ROW 3														
			CONN		P	1	B	P	EA	1	30-Aug-89		31-Dec-99		100	0	PROD
0067	408110008		TERMINAL DOUBLE TURRET														
			CONN		P	1	B	P	EA	2	01-Feb-89		31-Dec-99		100	0	PROD
0047	419141008		SWITCH "PIANO DIP" 8-POS														
			SWIT		P	1	B	P	EA	1	21-Oct-88		31-Dec-99		100	0	PROD
			U5														
0056	433112003		FUSE SLO-BLO 250V 1 AMP														
		4	FUSE		P	1	B	P	EA	1	07-Nov-88		31-Dec-99		100	0	PROD
			F1														
0048	433220001		FUSE PICO II 125V 10 AMP														
			FUSE		P	1	B	P	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			F2														
0057	434362002		FUSE CLIP FOR 1/4" FUSE														
			FUSE		P	1	B	P	EA	2	07-Nov-88		31-Dec-99		100	0	PROD
0070	454370002		SHUNT 2 POS														
			SOCK		P	1	B	P	EA	1	30-Aug-89		31-Dec-99		100	0	PROD
0058	454510005		HDR SOLD TAIL/MALE 5														
		4	CONN		P	1	B	P	EA	1	07-Nov-88		31-Dec-99		100	0	PROD
			J1														
0049	454611050		HDR SOLD TAIL/MALE 50														
			CONN		P	1	B	P	EA	1	11-Oct-88		31-Dec-99		100	0	PROD
			J3														
0061	719100016		PC BD PREASS'Y 9100-16														
		4	PCB		P	1	A	P	EA	1	07-Nov-88		31-Dec-99		100	0	FAB

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-16 COMPLETED BOARD 9100-16 UM: EA PC: 4 ECN: 1003 ASSEMBLY QTY: 1
ERC: P SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 06-Aug-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY	PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0040	SM227050186		IC 16-BIT MICROCONTR 80186																
		4		IC			P	B	1	EA	1		11-Oct-88		31-Dec-99		300	0	PROD
			GIVE TO SSD MANU.																

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-18 HI SPEED MEMORY BD 9100-18 UM: EA PC: 4 ECN: 1002 ASSEMBLY QTY: 1
ERC: E SRCE CODE: A TYPE: 1 ABC: D PL: P DATE: 23-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0053	106425103		CAP CERA MONO REEL .01UF									
			CAP	P 1 B P EA	75	16-Apr-90		31-Dec-99		100	0	PROD
			C1-C4,C6,C7,C9,C11-C15,C17-C26,C28,C29,C31,C32,C34,C36-C39,C41-C43,C46-C56,C58,C59,C61-C64,C66-C74,C76,C77,C79-C87,C89,C90,C93,C94									
0054	141838335		CAP TANT DIP REEL 3.3UF									
			CAP	P 1 B P EA	19	16-Apr-90		31-Dec-99		100	0	PROD
			C5,C8,C10,C16,C27,C30,C33,C35,C40,C44,C45,C57,C60,C65,C75,C78,C88,C91,C92									
0031	161225101		RES CARBON FILM 100 OHMS									
			RES	P 1 B P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
			R10,R11									
0033	161225102		RES CARBON FILM 1 K									
			RES	P 1 B P EA	6	23-Mar-90		31-Dec-99		100	0	PROD
			R7-R9,R14,R16,R17									
0032	161225103		RES CARBON FILM 10 K									
			RES	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			R12									
0034	161225512		RES CARBON FILM 5.1 K									
			RES	P 1 B P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
			R6,R13									
0035	161225820		RES CARBON FILM 82 OHMS									
			RES	P 1 B P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
			R2,R3									
0036	161335131		RES CARBON FILM 130 OHMS									
			RES	P 1 B P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
			R1,R5									
0041	190042222		RESISTOR NETWORK 2.2 K									
			RES	P 1 B P EA	4	23-Mar-90		31-Dec-99		100	0	PROD
			U1,U29,U106,U110									
0042	190042471		RESISTOR NETWORK 470 OHMS									
			RES	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			U38									
0030	200031032		IC HEX BUFF/DRIV SN7407N									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U96									
0013	200031046		IC HEX INVERTER SN74LS04N									
			IC	P 1 B P EA	2	16-Feb-90		31-Dec-99		100	0	PROD
			U79,U87									
0027	200031049		IC D-TYP FLOP SN74LS74N									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U95									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-18 HI SPEED MEMORY BD 9100-18 UM: EA PC: 4 ECN: 1002 ASSEMBLY QTY: 1
ERC: E SRCE CODE: A TYPE: 1 ABC: D PL: P DATE: 23-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0005	200031051		IC 2-INPUT NOR SN74LS02N									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U84									
0046	200031073		IC 2-IN POS OR SN74LS32N									
			IC	P 1 B P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
			U88,U94									
0052	200031086		IC 2-INPUT AND SN74LS08N									
			IC	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			U86									
0007	200032010		IC 2-INPUT NAND 74LS38PC									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U97									
0008	200041049		IC D-TYP FLOP SN74LS175N									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U101									
0012	200041054		IC DATA SELCTR SN74LS153N									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U82									
0028	200041062		IC DEC/DEMULTP SN74LS138N									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U81									
0045	200041139		IC DEC/MULTIPL SN74LS139N									
			IC	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			U104									
0002	200071001		IC 8 X BUFFER SN74LS240									
			IC	P 1 B P EA	3	16-Feb-90		31-Dec-99		100	0	PROD
			U99,U102,U103									
0003	200071007		IC BUFFER SN74LS244N									
			IC	P 1 B P EA	6	16-Feb-90		31-Dec-99		100	0	PROD
			U2,U30,U58,U68,U91, U98									
0001	200071245		IC BUS XCEIVER SN74LS245N									
			IC	P 1 B P EA	6	16-Feb-90		31-Dec-99		100	0	PROD
			U60-U63,U78,U107									
0050	200071373		IC D-TYP LATCH 74LS373N									
			IC	P 1 B P EA	5	23-Mar-90		31-Dec-99		100	0	PROD
			U3,U4,U31,U32,U59									
0048	200330008		IC 2-INPUT AND GATE 74F08									
			IC	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			U92									
0047	200333000		IC QUAD 2-IN NAND HCT00									
			IC	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			U80									
0049	200340074		IC D-TYPE POS FLOP 74F74									
			IC	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			U73									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-18 HI SPEED MEMORY BD 9100-18 UM: EA PC: 4 ECN: 1002 ASSEMBLY QTY: 1
ERC: E SRCE CODE: A TYPE: 1 ABC: D PL: P DATE: 23-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0017	200344131		IC DUAL D M-S FLOP 10H131									
			IC	P 1 A P EA	1	16-Aug-90		31-Dec-99		100	0	PROD
			U66									
0009	200344138		IC 3-TO-8 DECODER 138									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U85									
0051	200372374		IC 8-BIT REGIST 74LS374									
			IC	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			U57									
0011	200374374		IC D-TYP FLOP 74F374									
			IC	P 1 B P EA	6	16-Feb-90		31-Dec-99		100	0	PROD
			U13,U37,U64,U69-U71									
0026	200670373		IC LATCH 74F373PC									
			IC	P 1 B P EA	2	16-Feb-90		31-Dec-99		100	0	PROD
			U76,U77									
0018	204042004		IC 2-3-2-IN GATE MC10105P									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U40									
0014	204042007		IC QUAD TRANSL MC10124P									
			IC	P 1 A P EA	9	16-Feb-90		31-Dec-99		100	0	PROD
			U18,U19,U24,U25,U33-U36,U72									
0056	205271064		IC 8K X 8 RAM 7164S									
		4	IC	P 1 A P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
			U67,U90									
0010	205750168		IC 7-WIDE AND-OR-INV 16L8									
			IC	P 1 B P EA	2	16-Feb-90		31-Dec-99		100	0	PROD
			U83,U100									
0062	205791020		IC GATE ARRAY ACT1020									
		4	IC	P 1 A P EA	1	29-Mar-90		31-Dec-99		100	0	PROD
			PMS307A, REV.C (U89)									
0015	207244125		IC QUAD MECL-TTL 10H125									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U39									
0016	207340174		IC 4-TO-1 MULTIPLX 10174									
		4	IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U15									
0004	207470640		IC BUS TRANSCEIVER LS640									
			IC	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U105									
0040	240425746		DIODE ZENER 3.3V 1N746A									
			DIOD	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			CR3									
0019	253050817		DIODE HOT CARRIER 1N5817									
			DIOD	P 1 B P EA	2	16-Feb-90		31-Dec-99		100	0	PROD
			CR1,CR2									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-18 HI SPEED MEMORY BD 9100-18 UM: EA PC: 4 ECN: 1002 ASSEMBLY QTY: 1
ERC: E SRCE CODE: A TYPE: 1 ABC: D PL: P DATE: 23-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION / COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0055	270110003		TRANSISTOR NPN PN2222A XIST	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			Q1									
0065	290130010		DELAY LINE 10 N-SEC DELA	P 1 B P EA	1	29-Mar-90		31-Dec-99		100	0	PROD
			U14									
0037	300050001		CHOKE FERRITE SINGLE LEAD INDU	P 1 A P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
			L1,L2									
0006	399160014	4	SOCKET STACKABLE SIP-14 SOCK	P 1 * P EA	16	18-Jul-90		31-Dec-99		100	0	PROD
0020	399160016	4	SOCKET STACKABLE SIP-16 SOCK	P 1 * P EA	32	18-Jul-90		31-Dec-99		100	0	PROD
0070	400050028		SOCKET IC SOLD TAIL DIP-28 SOCK	P 1 B P EA	2	11-Apr-90		31-Dec-99		100	0	PROD
0059	400170020		SOCKET IC SOLD TAIL DIP-20 SOCK	P 1 B P EA	2	29-Mar-90		31-Dec-99		100	0	PROD
0061	400419084	4	IC SOCKET GRID TYPE 84-PIN SOCK	P 1 B P EA	1	29-Mar-90		31-Dec-99		100	0	PROD
0021	402610005	4	CONN CO-AX PC MTG SMB CONN	P 1 A P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			J112									
0022	403170026		HDR DBL ROW RT ANGL 26 CONN	P 1 B P EA	2	16-Feb-90		31-Dec-99		100	0	PROD
			J117,J120									
0023	403170034		HDR DBL ROW RT ANGL 34 CONN	P 1 B P EA	2	16-Feb-90		31-Dec-99		100	0	PROD
			J115,J116									
0024	403181003		HDR SINGL ROW 3 CONN	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			J50									
0039	433222005		FUSE PICO II 125V 2 AMP FUSE	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			F2									
0038	433225001		FUSE PICO II 125V 5 AMP FUSE	P 1 B P EA	1	23-Mar-90		31-Dec-99		100	0	PROD
			F1									
0025	454318012	4	HDR SOLD TAIL/MALE 12 CONN	P 1 B P EA	1	16-Feb-90		31-Dec-99		100	0	PROD
			U28									
0044	454370002		SHUNT 2 POS SOCK	P 1 B P EA	2	23-Mar-90		31-Dec-99		100	0	PROD
0060	510160001		GROUND LUG SPADE TYPE HDWR	P 1 B P EA	0	28-Mar-90		31-Dec-99		100	0	PROD
			QTY OF 6 TO BE SUPP- LIED BY PYRO. G1-G6									

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-18 HI SPEED MEMORY BD 9100-18 UM: EA PC: 4 ECN: 1002 ASSEMBLY QTY: 1
ERC: E SRCE CODE: A TYPE: 1 ABC: D PL: P DATE: 23-Jul-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0057	719100018		PC BD PREASS'Y 9100-18														
		4	PCB	P	1	A	P		EA	1	23-Mar-90		31-Dec-99		100	0	FAB

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-22 COMPLETED BOARD 9100-22 UM: EA PC: 4 ECN: 1007 ASSEMBLY QTY: 1
ERC: V SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION / CODE / COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0015	106415103	4	CAP CERA MONO 100V .01UF CAP C1-C3,C5,C7-C15,C17 C19,C22-C26,C28-C36 C38-C40,C42-C48,C50 C52-C59,C61-C63		P	1	B	P	EA	51	21-Sep-90		31-Dec-99		100	0	PROD
0024	146134476		CAP MINI ALUM 20% 47 UF CAP C27		P	1	B	P	EA	1	18-Apr-88		31-Dec-99		100	0	PROD
0016	146424106		CAP MINI ALUM 20% 10 UF CAP C4,C6,C16,C18,C20 C21,C37,C41,C49,C51		P	1	B	P	EA	10	29-Apr-88		31-Dec-99		100	0	PROD
0036	161225161		RES CARBON FILM 160 OHMS RES R27,R31,R42,R43		P	1	B	P	EA	4	11-May-88		31-Dec-99		100	0	PROD
0035	161225271		RES CARBON FILM 270 OHMS RES R28,R32,R45,R46		P	1	B	P	EA	4	11-May-88		31-Dec-99		100	0	PROD
0042	161225750		RES CARBON FILM 75 OHMS RES U23(8X), U24(8X) U25(8X)		P	1	B	P	EA	24	03-Oct-88		31-Dec-99		100	0	PROD
0006	161225820		RES CARBON FILM 82 OHMS RES R2,R3,R5,R8,R9,R12 R13,R16,R17,R20,R22 R23,R26,R29,R33,R40 R48		P	1	B	P	EA	17	11-May-89		31-Dec-99		100	0	PROD
0005	161335131		RES CARBON FILM 130 OHMS RES R1,R4,R6,R7,R10,R11 R14,R15,R18,R19,R21 R24,R25,R30,R34,R39 R41		P	1	B	P	EA	17	11-May-88		31-Dec-99		100	0	PROD
0043	190042102		RESISTOR NETWORK 1 K RES U100,U101,U102		P	1	B	P	EA	3	03-Oct-88		31-Dec-99		100	0	PROD
0046	190042471		RESISTOR NETWORK 470 OHMS RES U33,U36,U38,U41		P	1	B	P	EA	4	22-Nov-88		31-Dec-99		100	0	PROD
0007	190102001		RES NETWORK 220/330 OHMS RES U16,U17,U19,U21,U27 U31		P	1	B	P	EA	6	22-Feb-89		31-Dec-99		100	0	PROD
0045	200000105	4	IC SPECIAL OR/NOR 105 IC U34,U35,U37,U39,U40 U42		P	1	B	P	EA	6	04-Jan-89		31-Dec-99		100	0	PROD

EFFECTIVITY DATE: 26-Sep-90 S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100-22 COMPLETED BOARD 9100-22 UM: EA PC: 4 ECN: 1007 ASSEMBLY QTY: 1
ERC: V SRCE CODE: A TYPE: 1 ABC: B PL: P DATE: 21-Sep-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S T S A P C Y P B L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0029	200344102		IC QUAD 2-IN NOR 10H102											
			IC		P 1 B P	EA	8	29-Apr-88		31-Dec-99		100	0	PROD
			U4,U5,U6,U7,U10,U11 U12,U13											
0004	207244125		IC QUAD MECL-TTL 10H125											
			IC		P 1 B P	EA	5	22-Feb-89		31-Dec-99		100	0	PROD
			U26,U28-30,U32											
0030	235010005		DIODE RECTIFIER 1N4005											
			DIOD		P 1 B P	EA	1	29-Apr-88		31-Dec-99		100	0	PROD
			CR1											
0017	300050001		CHOKE FERRITE SINGLE LEAD											
			INDU		P 1 A P	EA	2	11-Mar-88		31-Dec-99		100	0	PROD
			L1,L2											
0012	402610005		CONN CO-AX PC MTG SMB											
		4	CONN		P 1 A P	EA	4	19-May-89		31-Dec-99		100	0	PROD
0014	403170034		HDR DBL ROW RT ANGL 34											
			CONN		P 1 B P	EA	2	11-Mar-88		31-Dec-99		100	0	PROD
			J6,J7											
0021	405764112		SOCKET SINGLE WIRE 12-POS											
			SOCK		P 1 B P	EA	12	14-Apr-88		31-Dec-99		100	0	PROD
			J1-J4,U23-U25											
0023	408110008		TERMINAL DOUBLE TURRET											
			CONN		P 1 B P	EA	2	15-Apr-88		31-Dec-99		100	0	PROD
			TP'S											
0031	433221004		FUSE PICO II 125V 1 AMP											
			FUSE		P 1 B P	EA	1	29-Apr-88		31-Dec-99		100	0	PROD
			F1											
0037	433225001		FUSE PICO II 125V 5 AMP											
			FUSE		P 1 B P	EA	1	22-Feb-89		31-Dec-99		100	0	PROD
			F2											
0022	505112140		HEAT SINK											
			HEAT		P 1 B P	EA	4	14-Apr-88		31-Dec-99		100	0	PROD
			U15,U18,U20,U22											
0039	528055016		PLUG(POTTING BASE) DIP-16											
			CONN		P 1 B P	EA	3	08-Aug-88		31-Dec-99		100	0	PROD
0018	719100022		PC BD PREASS'Y 9100-22											
		4	PCB		P 1 A P	EA	1	11-Mar-88		31-Dec-99		100	0	FAB
0025	SM205624141		IC 8-BIT SHIFT REG 100141											
			IC		P 1 A P	EA	4	18-Apr-88		31-Dec-99		100	0	PROD
			U15,U18,U20,U22											
0026	SM207124112		IC QUAD LINE DRIVER 112											
			IC		P 1 B P	EA	2	18-Apr-88		31-Dec-99		100	0	PROD

NOTES:

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100MF

MAIN FRAME ASS'Y 9100 UM: EA PC: 4 ECN: 1001 ASSEMBLY QTY: 1
ERC: G SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 17-Jan-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.CODE	DESCRIPTION COM.CD	S T S A P C Y P B L UM	EXTENDED QTY PER	START DATE	START S/N	CLOSE DATE	CLOSE S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0007	521400004		SPACER ROUND #4 1/8									
			HDWR	P 1 B P EA	6	21-Feb-89		31-Dec-99		100	0	PROD
0008	530301131		HANDLE FOR RACK PANEL									
		4	FAB	P 1 B P EA	2	21-Feb-89		31-Dec-99		100	0	FAB
0009	530500015		19" RACK MTG ENCLOSURE									
		4	FAB	P 1 A P EA	1	21-Feb-89		31-Dec-99		100	0	SSD
0010	550140140		SCREW PAN HD M4X40									
		4	HDWR	P 1 B P EA	4	21-Feb-89		31-Dec-99		100	0	PROD
0011	550140206		SCREW PAN HD SLOT M4X6									
		4	HDWR	P 1 B P EA	8	21-Feb-89		31-Dec-99		100	0	PROD
0012	550150510		SCREW FLAT HD PHIL M5X10									
		4	HDWR	P 1 B P EA	4	21-Feb-89		31-Dec-99		100	0	PROD
0013	554140002		SCREW METRIC PHIL PAN HD									
		4	HDWR	P 1 B P EA	4	21-Feb-89		31-Dec-99		100	0	PROD
0022	555100003		NUT SQUARE 4-40									
		4	HDWR	P 1 B P EA	4	21-Feb-89		31-Dec-99		100	0	PROD
0023	560440006		SCREW PHILIPS 4-40X3/8									
			HDWR	P 1 B P EA	2	21-Feb-89		31-Dec-99		100	0	PROD
0024	560440007		SCREW PHILIPS 4-40X7/16									
			HDWR	P 1 B P EA	4	21-Feb-89		31-Dec-99		100	0	PROD
0015	560632006		SCREW PHILIPS 6-32X3/8									
			HDWR	P 1 B P EA	10	21-Feb-89		31-Dec-99		100	0	PROD
0016	567440006		SCREW FLAT PHIL 4-40X3/8									
			HDWR	P 1 B P EA	8	21-Feb-89		31-Dec-99		100	0	PROD
0017	575610002		WASHER FLAT REG OD SIZE 6									
			HDWR	P 1 B P EA	8	21-Feb-89		31-Dec-99		100	0	PROD
0018	575802005		WASHER NYLON #8									
		4	HDWR	P 1 B P EA	4	21-Feb-89		31-Dec-99		100	0	PROD
0025	576410001		WASHER SPLIT LOCK SIZE 4									
			HDWR	P 1 B P EA	6	21-Feb-89		31-Dec-99		100	0	PROD
0019	589203318		AC PWR CORD 3-COND									
		4	WIRE	P 1 B P EA	1	21-Feb-89		31-Dec-99		100	0	PROD
0026	597910001		SHIPPING CARTON 9100									
		4	SHIP	P 1 B P EA	1	16-Mar-89		31-Dec-99		100	0	PROD
0027	597910002		SHIPPING CARTON BOT CAP 9100									
		4	SHIP	P 1 A P EA	1	16-Mar-89		31-Dec-99		100	0	PROD
0028	597910003		SHIPPING CARTON TOP CAP 9100									
		4	SHIP	P 1 A P EA	1	16-Mar-89		31-Dec-99		100	0	PROD
0030	597910012		SHIPPING BOX 9100 ACCESSORIES									
		4	SHIP	P 1 B P EA	1	16-Mar-89		31-Dec-99		100	0	PROD
0020	709100021		TIE-DOWN BAR FOR 9100									
		4	FAB	P 1 B P EA	3	21-Feb-89		31-Dec-99		100	0	FAB
0021	709400071		REAR PANEL FOOT 9400									
		4	FAB	P 1 B P EA	4	21-Feb-89		31-Dec-99		100	0	FAB
0004	9100-10	Y	REAR PNL ASS'Y 9100-10									
		4	ASSY	A 1 A P EA	1	30-Jul-86		31-Dec-99		600	0	SSDSUB

EFFECTIVITY DATE: 26-Sep-90

S I N G L E L E V E L B I L L S O F M A T E R I A L

PARENT PART: 9100MF MAIN FRAME ASS'Y 9100 UM: EA PC: 4 ECN: 1001 ASSEMBLY QTY: 1
ERC: G SRCE CODE: A TYPE: 1 ABC: A PL: P DATE: 17-Jan-90

ITEM NO	COMPONENT PART NUMBER	ERC PROD.	DESCRIPTION CODE	COM.CD	S C	T Y	S P	A B	P L	UM	EXTENDED QTY PER	START DATE	S/N	CLOSE DATE	S/N	OPR SEQ	LT OFF	STORES ACCOUNT
0002	9100-8	U 4	CARD CAGE/PWR SUPPLY ASSY		A	1	A	P	P	EA	1	30-Jul-86		31-Dec-99		600	0	SSDSUB

NOTES:

END OF REPORT

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